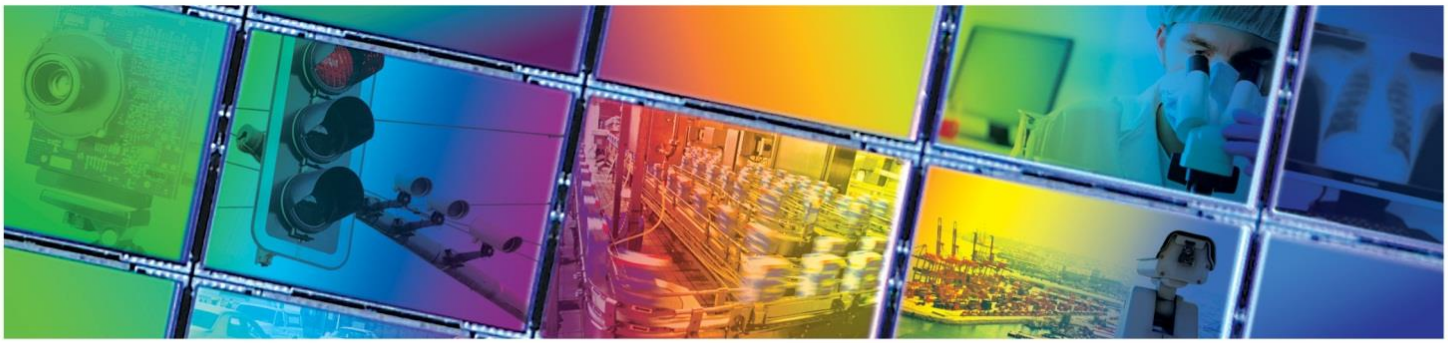
ON Semiconductor®

KAI-2020 IMAGE SENSOR

1600 (H) X 1200 (V) INTERLINE CCD IMAGE SENSOR



JUNE 9, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.1 PS-0017

TABLE OF CONTENTS

TABLE OF FIGURES

Summary Specification

KAI-2020 Image Sensor

DESCRIPTION

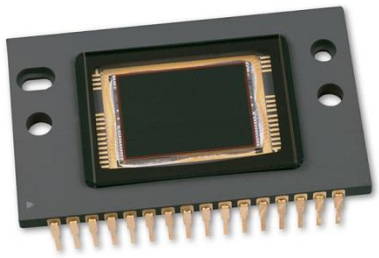
The KAI-2020 Image Sensor is a high performance 2-million pixel sensor designed for a wide range of medical, scientific and machine vision applications. The 7.4 µm square pixels with microlenses provide high sensitivity and the large full well capacity results in high dynamic range. The split horizontal register offers a choice of single or dual output allowing either 18 or 35 frame per second (fps) video rate for the progressively scanned images. Also included is a fast line dump for sub-sampling at higher frame rates. The vertical overflow drain structure provides antiblooming protection and enables electronic shuttering for precise exposure control. Other features include low dark current, negligible lag and low smear.

FEATURES

- High resolution
- High sensitivity
- High dynamic range
- Low noise architecture
- High frame rate
- Binning capability for higher frame rate
- Electronic shutter

APPLICATIONS

- Intelligent Transportation Systems
- Machine Vision
- Scientific
- Surveillance



Parameter	Typical Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	1640 (H) x 1214 (V)
Number of Effective Pixels	1608 (H) x 1208 (V)
Number of Active Pixels	1600 (H) x 1200 (V)
Pixel Size	7.4 µm (H) x 7.4 µm (V)
Active Image Size	11.84 mm (H) x 8.88 mm (V) 14.80 mm (diagonal)
Aspect Ratio	4:3
Number of Outputs	1 or 2
Saturation Signal 40 MHz 20 MHz	 20,000 e^- 40,000 e^-
Output Sensitivity	30 µV/e^-
Quantum Efficiency -ABA (460 nm) -CBA (620 nm, 540 nm, 460 nm)	 55% 31%, 37%, 41%
Readout Noise 40 MHz 20 MHz	 20 electrons 16 electrons
Dynamic Range 40 MHz 20 MHz	 60 dB 68 dB
Dark Current	< 0.5 nA/cm^2
Maximum Pixel Clock Speed	40 MHz
Maximum Frame Rate Dual Output Single Output	 35 fps 18 fps
Package type	32 pin CerDIP
Package Size	0.790” [20.07 mm] width 1.300” [33.02 mm] length
Package pin spacing	0.070”
Cover Glass	AR coated, 2 sides

Parameters above are specified at T = 40 °C unless otherwise noted.

Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H0466	KAI- 2020-AAA-CF-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Quartz Cover Glass (no coatings), Engineering Sample	KAI-2020 Serial Number
4H0465	KAI- 2020-AAA-CF-BA	Monochrome, No Microlens, CERDIP Package (sidebrazed), Quartz Cover Glass (no coatings), Standard Grade	
4H0458	KAI- 2020-AAA-CR-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Engineering Sample	
4H0457	KAI- 2020-AAA-CR-BA	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Standard Grade	
4H0794	KAI- 2020-ABA-CD-AE	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	KAI-2020M Serial Number
4H0793	KAI- 2020-ABA-CD-BA	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Standard Grade	
4H0796	KAI- 2020-ABA-CR-AE	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Engineering Sample	
4H0795	KAI- 2020-ABA-CR-BA	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Standard Grade	
4H0460	KAI- 2020-CBA-CD-AE	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	KAI-2020CM Serial Number
4H0459	KAI- 2020-CBA-CD-BA	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Standard Grade	
4H0844	KAI- 2020-CBA-CR-AE	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Engineering Sample	
4H0843	KAI- 2020-CBA-CR-BA	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Standard Grade	
4H0691	KEK-4H0691-KAI-2001/2020-12-20	Evaluation Board, 12 Bit, 20 MHz (Complete Kit)	n/a
4H0692	KEK-4H0692-KAI-2001/2020-10-40	Evaluation Board, 10 Bit, 40 MHz (Complete Kit)	n/a

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

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Device Description

ARCHITECTURE

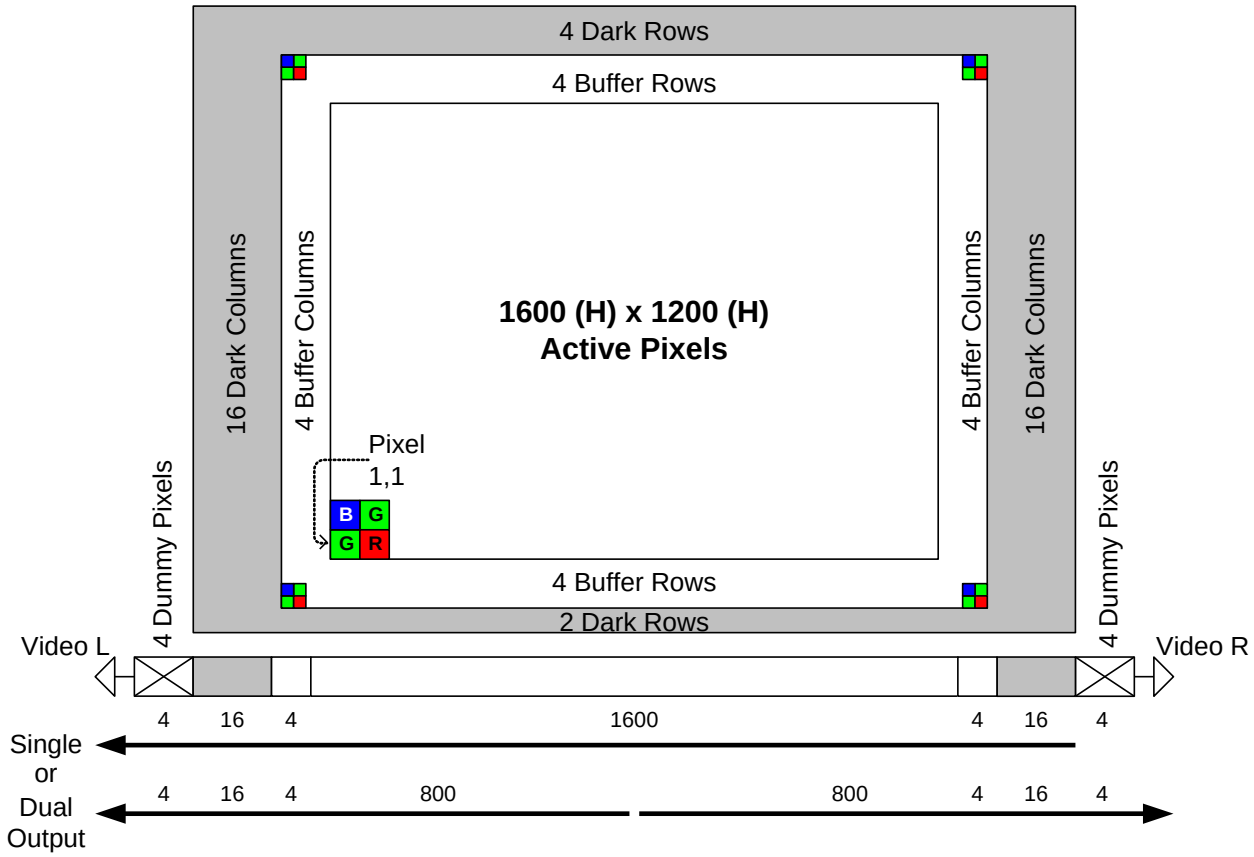


Figure 1: Sensor Architecture

There are 2 light shielded rows followed 1208 photoactive rows and finally 4 more light shielded rows. The first 4 and the last 4 photoactive rows are buffer rows giving a total of 1200 lines of image data.

In the single output mode all pixels are clocked out of the Video L output in the lower left corner of the sensor. The first 4 empty pixels of each line do not receive charge from the vertical shift register. The next 16 pixels receive charge from the left light shielded edge followed by 1608 photosensitive pixels and finally 16 more light shielded pixels from the right edge of the sensor. The first and last 4 photosensitive pixels are buffer pixels giving a total of 1600 pixels of image data.

In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is clocked out Video L and the right half of the image is clocked out Video R. Each row consists of 4 empty pixels followed by 16 light shielded pixels followed by 800 photosensitive pixels. When reconstructing the image, data from Video R will have to be reversed in a line buffer and appended to the Video L data.

Pixel

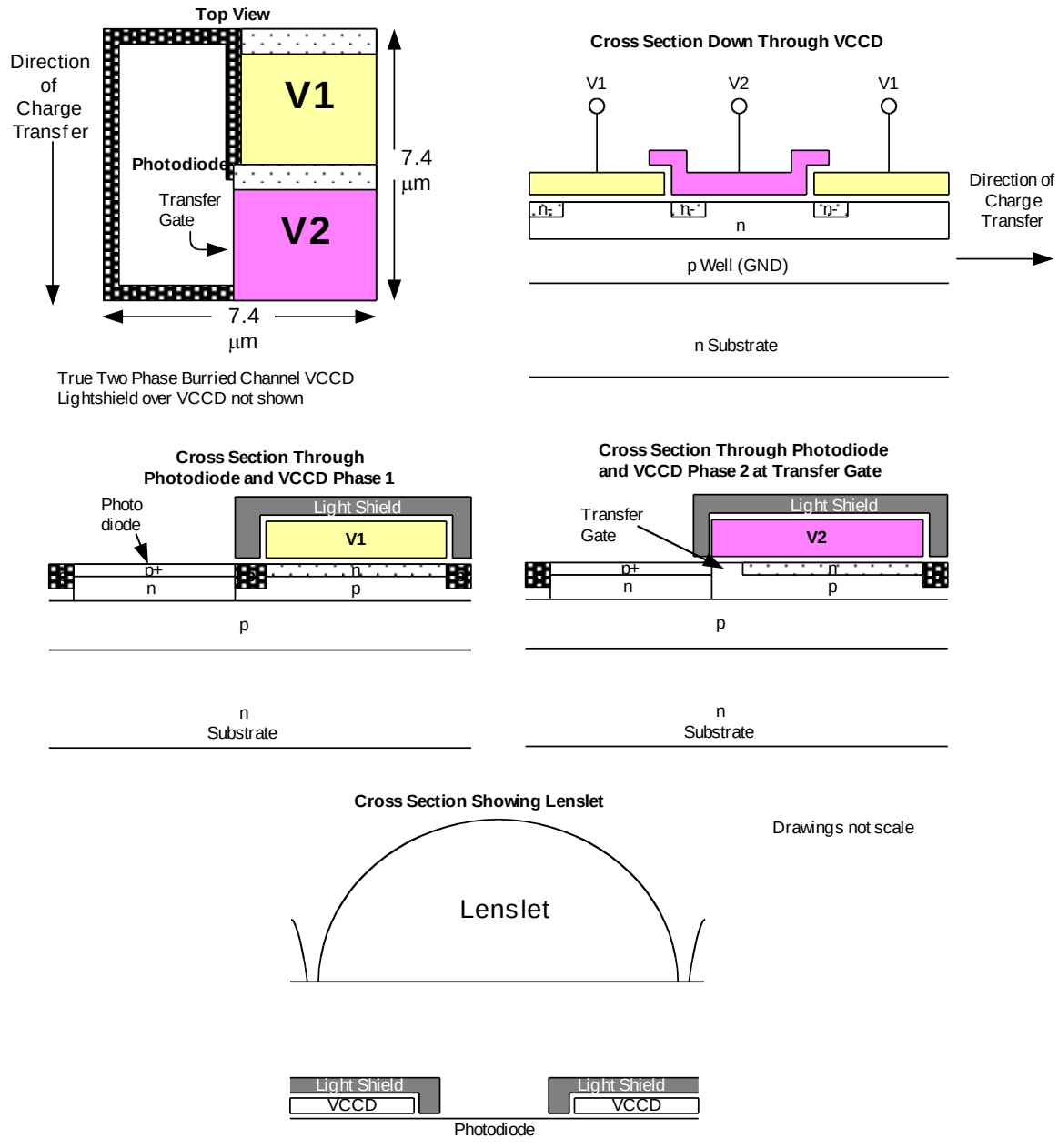


Figure 2: Pixel Architecture

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

Vertical to Horizontal Transfer

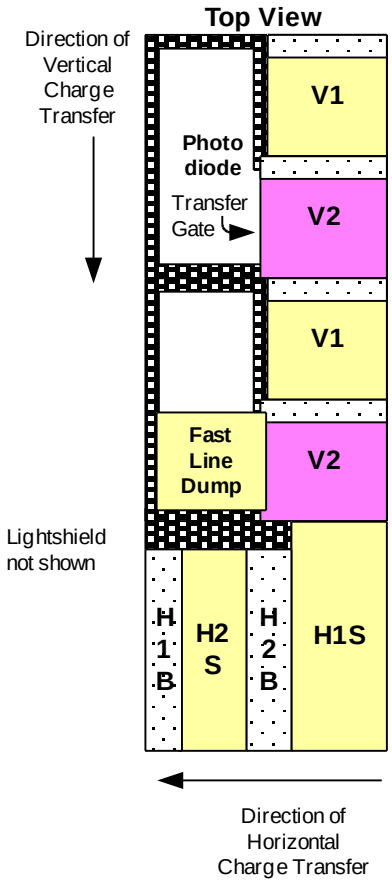


Figure 3: Vertical to Horizontal Transfer Architecture

When the V1 and V2 timing inputs are pulsed, charge in every pixel of the VCCD is shifted one row towards the HCCD. The last row next to the HCCD is shifted into the HCCD. When the VCCD is shifted, the timing signals to the HCCD must be stopped. H1 must be stopped in the high state and H2 must be stopped in the low state. The HCCD clocking may begin T_{HD} µs after the falling edge of the V1 and V2 pulse.

Charge is transferred from the last vertical CCD phase into the H1S horizontal CCD phase. Refer to Figure 27 for an example of timing that accomplishes the vertical to horizontal transfer of charge.

If the fast line dump is held at the high level (FDH) during a vertical to horizontal transfer, then the entire line is removed and not transferred into the horizontal register.

Horizontal Register to Floating Diffusion

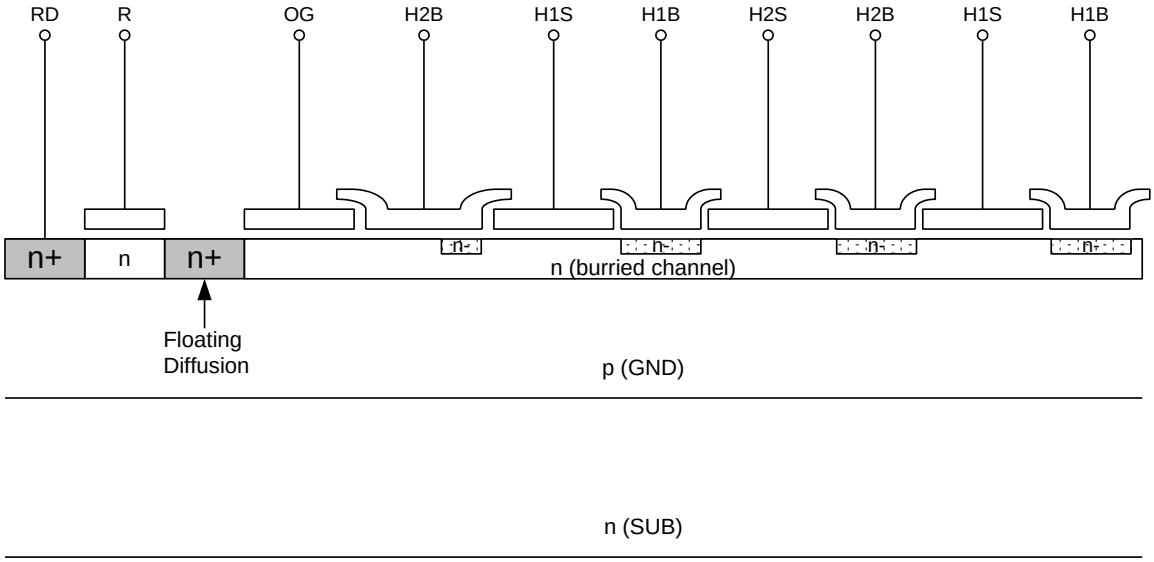


Figure 4: Horizontal Register to Floating Diffusion Architecture

The HCCD has a total of 1648 pixels. The 1640 vertical shift registers (columns) are shifted into the center 1640 pixels of the HCCD. There are 4 pixels at both ends of the HCCD, which receive no charge from a vertical shift register. The first 4 clock cycles of the HCCD will be empty pixels (containing no electrons). The next 16 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. The next 1608 clock cycles will contain photo-electrons (image data). Finally, the last 16 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. Of the 16 dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns. Only use the center 14 columns of the 16 column dark reference.

When the HCCD is shifting valid image data, the timing inputs to the electronic shutter (SUB), VCCD (V1, V2), and fast line dump (FD) should be not be pulsed. This prevents unwanted noise from being introduced. The HCCD is a type of charge coupled device known as a pseudo-two phase CCD. This type of CCD has the ability to shift charge in two directions. This allows the entire image to be shifted out to the video L output, or to the video R output (left/right image reversal). The HCCD is split into two equal halves of 824 pixels each. When operating the sensor in single output mode the two halves of the HCCD are shifted in the same direction. When operating the sensor in dual output mode the two halves of the HCCD are shifted in opposite directions. The direction of charge transfer in each half is controlled by the H1BL, H2BL, H1BR, and H2BR timing inputs.

Horizontal Register Split

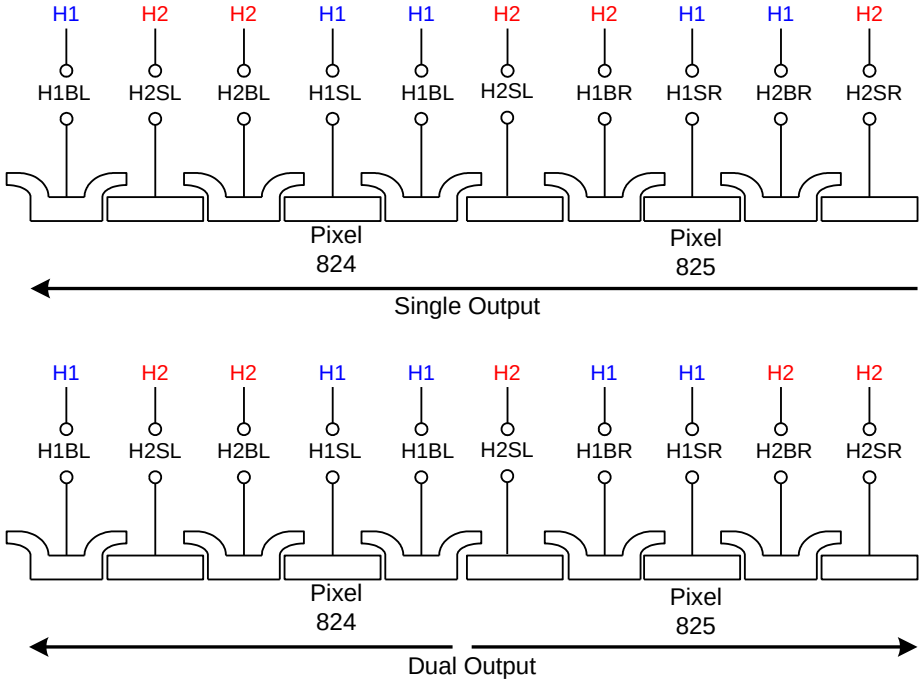


Figure 5: Horizontal Register

Single Output Operation

When operating the sensor in single output mode all pixels of the image sensor will be shifted out the Video L output (pin 31). To conserve power and lower heat generation the output amplifier for Video R may be turned off by connecting VDDR (pin 24) and VOUTR (pin 24) to GND (zero volts).

The H1 timing from the timing diagrams should be applied to H1SL, H1BL, H1SR, H2BR, and the H2 timing should be applied to H2SL, H2BL, H2SR, and H1BR. In other words, the clock driver generating the H1 timing should be connected to pins 4, 3, 13, and 15. The clock driver generating the H2 timing should be connected to pins 5, 2, 12, and 14. The horizontal CCD should be clocked for 4 empty pixels plus 16 light shielded pixels plus 1608 photoactive pixels plus 16 light shielded pixels for a total of 1644 pixels.

Dual Output Operation

In dual output mode the connections to the H1BR and H2BR pins are swapped from the single output mode to change the direction of charge transfer of the right side horizontal shift register. In dual output mode both VDDL and VDDR (pins 25, 24) should be connected to 15 V. The H1 timing from the timing diagrams should be applied to H1SL, H1BL, H1SR, H1BR, and the H2 timing should be applied to H2SL, H2BL, H2SR, and H2BR. The clock driver generating the H1 timing should be connected to pins 4, 3, 13, and 14. The clock driver generating the H2 timing should be connected to pins 5, 2, 12, and 15. The horizontal CCD should be clocked for 4 empty pixels plus 16 light shielded pixels plus 804 photoactive pixels for a total of 824 pixels. If the camera is to have the option of dual or single output mode, the clock driver signals sent to H1BR and H2BR may be swapped by using a relay. Another alternative is to have two extra clock drivers for H1BR and H2BR and invert the signals in the timing logic generator. If two extra clock drivers are used, care must be taken to ensure the rising and falling edges of the H1BR and H2BR clocks occur at the same time (within 3 ns) as the other HCCD clocks.

Output

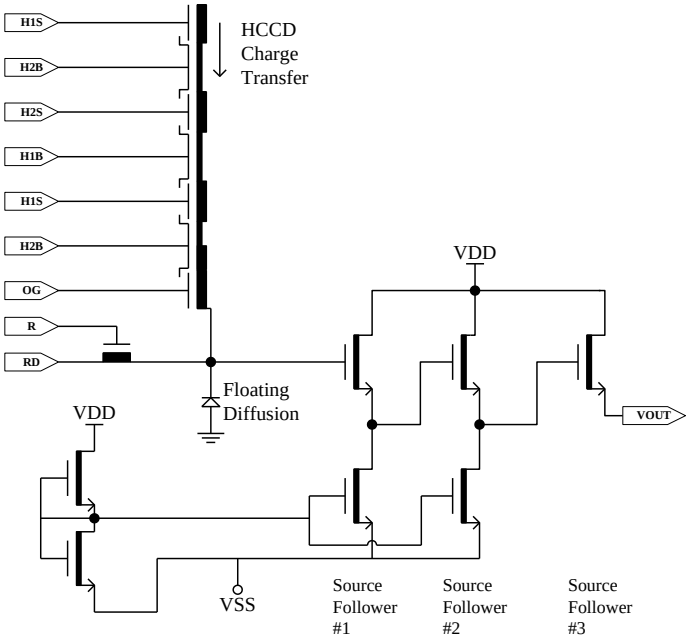


Figure 6: Output Architecture

Charge packets contained in the horizontal register are dumped pixel by pixel onto the floating diffusion (fd) output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential charge is determined by the expression $\Delta Vfd=\Delta Q/Cfd$.. A three-stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of microvolts per electron ($\mu V/e^-$). After the signal has been sampled off chip, the reset clock (R) removes the charge from the floating diffusion and resets its potential to the reset drain voltage (RD).

When the image sensor is operated in the binned or summed interlaced modes there will be more than 20,000 electrons in the output signal. The image sensor is designed with a 30 µV/e charge to voltage conversion on the output. This means a full signal of 20,000 electrons will produce a 600 mV change on the output amplifier. The output amplifier was designed to handle an output swing of 600 mV at a pixel rate of 40 MHz. If 40,000 electron charge packets are generated in the binned or summed interlaced modes then the output amplifier output will have to swing 1200 mV. The output amplifier does not have enough bandwidth (slew rate) to handle 1200 mV at 40 MHz. Hence, the pixel rate will have to be reduced to 20 MHz if the full dynamic range of 40,000 electrons is desired.

The charge handling capacity of the output amplifier is also set by the reset clock voltage levels. The reset clock driver circuit is very simple if an amplitude of 5 V is used. But the 5 V amplitude restricts the output amplifier charge capacity to 20,000 electrons. If the full dynamic range of 40,000 electrons is desired then the reset clock amplitude will have to be increased to 7 V.

If you only want a maximum signal of 20,000 electrons in binned or summed interlaced modes, then a 40 MHz pixel rate with a 5 V reset clock may be used. The output of the amplifier will be unpredictable above 20,000 electrons so be sure to set the maximum input signal level of your analog to digital converter to the equivalent of 20,000 electrons (600 mV).

The following table summarizes the previous explanation on the output amplifier's operation. Certain trade-offs can be made based on application needs such as Dynamic Range or Pixel frequency.

Pixel Freq. (MHz)	Reset Clock Amplitude (V)	Output Gate (V)	Saturation Signal (mV)	Saturation Signal (Ke^-)	Dynamic Range (dB)	Notes
40	5	-2.0	600	20	60	
20	5	-2.0	600	20	62	
20	7	-3	1200	40	68	
20	7	-3	2400	80	74	1

Notes:
1. 80,000 electrons achievable in summed interlaced or binning modes.

ESD Protection

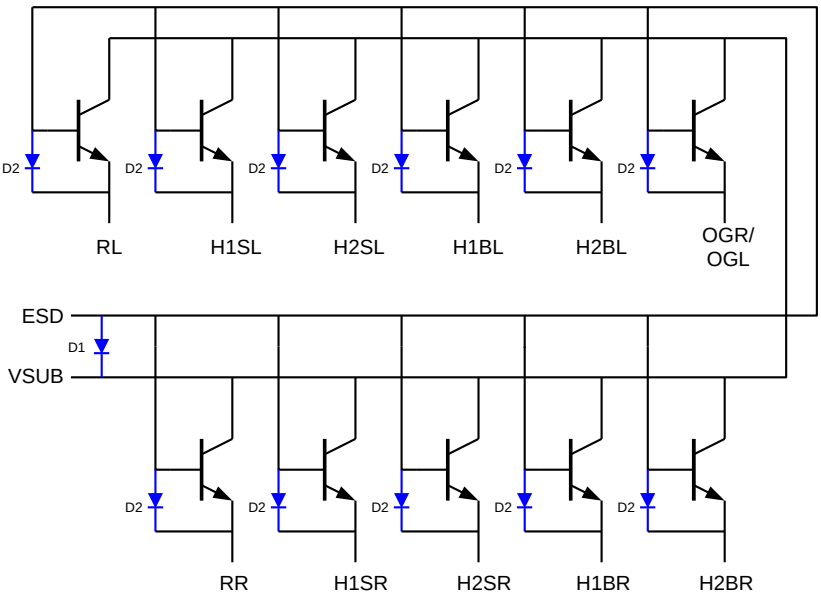


Figure 7: ESD Protection

The ESD protection on the KAI-2020 is implemented using bipolar transistors. The substrate (VSUB) forms the common collector of all the ESD protection transistors. The ESD pin is the common base of all the ESD protection transistors. Each protected pin is connected to a separate emitter as shown in Figure 7.

The ESD circuit turns on if the base-emitter junction voltage exceeds 17 V. Care must be taken while operating the image sensor, especially during the power on sequence, to not forward bias the base-emitter or base-collector junctions. If it is possible for the camera power up sequence to forward bias these junctions then diodes D1 and D2 should be added to protect the image sensor. Put one diode D1 between the ESD and VSUB pins. Put one diode D2 on each pin that may forward bias the base-emitter junction. The diodes will prevent large currents from flowing through the image sensor.

Note that diodes D1 and D2 are added external to the KAI-2020. These diodes are optional in camera design.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

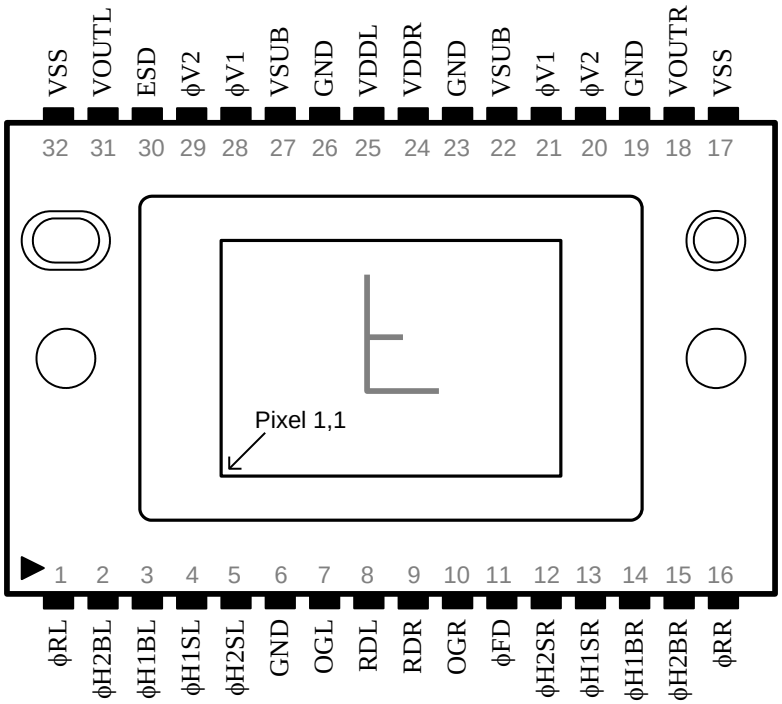


Figure 8: Package Pin Designations – Top View

Pin	Name	Description
1	φRL	Reset Gate, Left
2	φH2BL	H2 Barrier, Left
3	φH1BL	H1 Barrier, Left
4	φH1SL	H1 Storage, Left
5	φH2SL	H2 Storage, Left
6	GND	Ground
7	OGL	Output Gate, Left
8	RDL	Reset Drain, Left
9	RDR	Reset Drain, Right
10	OGR	Output Gate, Right
11	FD	Fast Line Dump Gate
12	φH2SR	H2 Storage, Right
13	φH1SR	H1 Storage, Right
14	φH1BR	H1 Barrier, Right
15	φH2BR	H2 Barrier, Right
16	φRR	Reset Gate, Right

Pin	Name	Description
32	VSS	Output Amplifier Return
31	VOUTL	Video Output, Left
30	ESD	ESD
29	φV2	Vertical Clock, Phase 2
28	φV1	Vertical Clock, Phase 1
27	VSUB	Substrate
26	GND	Ground
25	VDDL	Vdd, Left
24	VDDR	Vdd, Right
23	GND	Ground
22	VSUB	Substrate
21	φV1	Vertical Clock, Phase 1
20	φV2	Vertical Clock, Phase 2
19	GND	Ground
18	VOUTR	Video Output, Right
17	VSS	Output Amplifier Return

The pins are on a 0.07” spacing

Imaging Performance

TYPICAL OPERATIONAL CONDITIONS

Unless otherwise noted, Imaging Performance Specifications are measured using the following conditions:

Description	Condition	Notes
Frame time	237 msec	1
Horizontal clock frequency	10 MHz	
Light Source (LED)	Continuous red, green and blue illumination centered at 450, 530 and 650 nm	2, 3
Operation	Nominal operating voltages and timing	

Notes:

1. Electronic shutter is not used. Integration time equals frame time.
2. LEDs used: Blue: Nichia NLPB500, Green: Nichia NSPG500S and Red: HP HLMP-8115.
3. For monochrome sensor, only green LED used.

SPECIFICATIONS

All Configurations

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature(s) Tested At (°C)	Notes
Dark Center Uniformity		n/a	n/a	20	e-rms	Die	27, 40	
Dark Global Uniformity		n/a	n/a	5.0	mVpp	Die	27, 40	
Global Uniformity		n/a	2.5	5.0	%rms	Die	27, 40	1
Global Peak to Peak Uniformity	PRNU	n/a	10	20	%pp	Die	27, 40	1
Center Uniformity		n/a	1.0	2.0	%rms	Die	27, 40	1
Maximum Photoresponse Nonlinearity	NL	n/a	2		%	Design		2,3
Maximum Gain Difference Between Outputs	□G	n/a	10		%	Design		2,3
Max. Signal Error due to Nonlinearity Difference	□NL	n/a	1		%	Design		2,3
Horizontal CCD Charge Capacity	HNe	n/a	100	n/a	ke^-	Design		
Vertical CCD Charge Capacity	VNe	n/a	50	n/a	ke^-	Die		
Photodiode Charge Capacity (20 MHz)	PNe	38	40	n/a	ke^-	Die		
Photodiode Charge Capacity (40 MHZ)	PNe	19	20	n/a	ke^-	Die		
Horizontal CCD Charge Transfer Efficiency	HCTE	0.99999	n/a	n/a		Design		
Vertical CCD Charge Transfer Efficiency	VCTE	0.99999	n/a	n/a		Design		
Photodiode Dark Current	Ipd	n/a	40	350	$e/p/s$	Die	40	
Photodiode Dark Current	Ipd	n/a	0.01	0.1	nA/cm^2	Die	40	
Vertical CCD Dark Current	Ivd	n/a	400	1711	$e/p/s$	Die	40	
Vertical CCD Dark Current	Ivd	n/a	0.12	0.5	nA/cm^2	Die	40	
Image Lag	Lag	n/a	<10	50	e^-	Design		
Antiblooming Factor	Xab	100	300	n/a		Design		
Vertical Smear	Smr	n/a	80	75	dB	Design		
Sensor Read Noise (20MHz)	n_{e-T}		16		e^-rms	Design		
Sensor Read Noise (40MHz)	n_{e-T}		20		e^-rms	Design		
Dynamic Range (20MHz & 40 MHZ)	DR		68 60		dB	Design		4
Output Amplifier DC Offset	V_{odc}	4	8.5	14	V	Die		
Output Amplifier Bandwidth	F_{-3db}		140		MHz	Design		
Output Amplifier Impedance	R_{OUT}	100	130	200	Ohms	Die		
Output Amplifier Sensitivity	ΔV/ΔN		30		$\mu V/e^-$	Design		

KAI-2020-ABA Configuration

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature(s) Tested At (°C)	Notes
Peak Quantum Efficiency	QE_{max}	45	55	n/a	%	Design		
Peak Quantum Efficiency Wavelength	λQE	n/a	460	n/a	nm	Design		

KAI-2020-CBA Configuration

Description		Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature(s) Tested At (°C)	Notes
Peak Quantum Efficiency	Blue Green Red	QE_{max}		41 37 31	n/a	%	Design		
Peak Quantum Efficiency Wavelength	Blue Green Red	λQE	n/a	460 540 620	n/a	nm	Design		

n/a: not applicable

Notes:
1. For KAI-2020-CBA, per color
2. Value is over the range of 10% to 90% of photodiode saturation.
3. Value is for the sensor operated without binning
4. Uses 20LOG(PNe/n_{e-T})

Typical Performance Curves

QUANTUM EFFICIENCY

Monochrome with Microlens

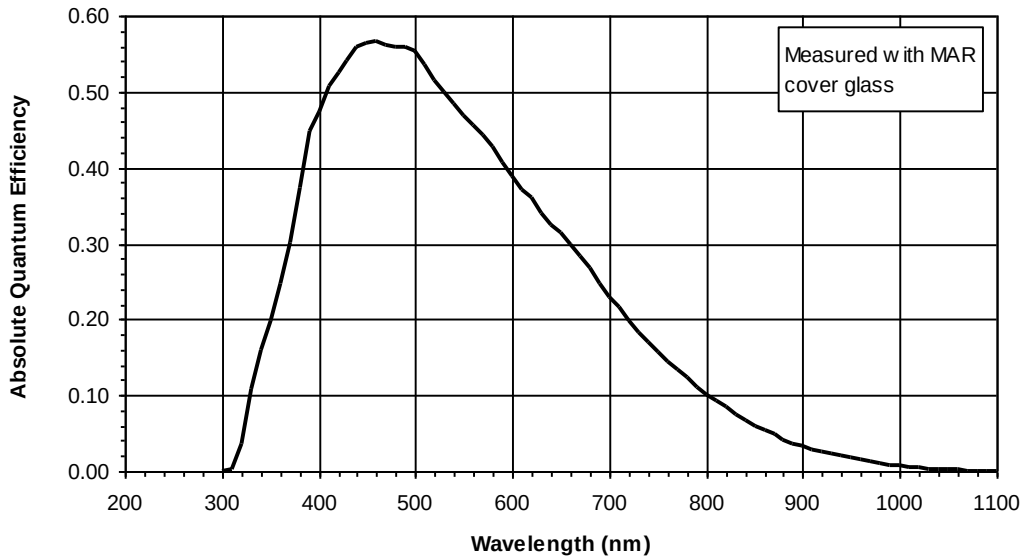


Figure 9: Monochrome with Microlens Quantum Efficiency

Monochrome without Microlens

Without coverglass

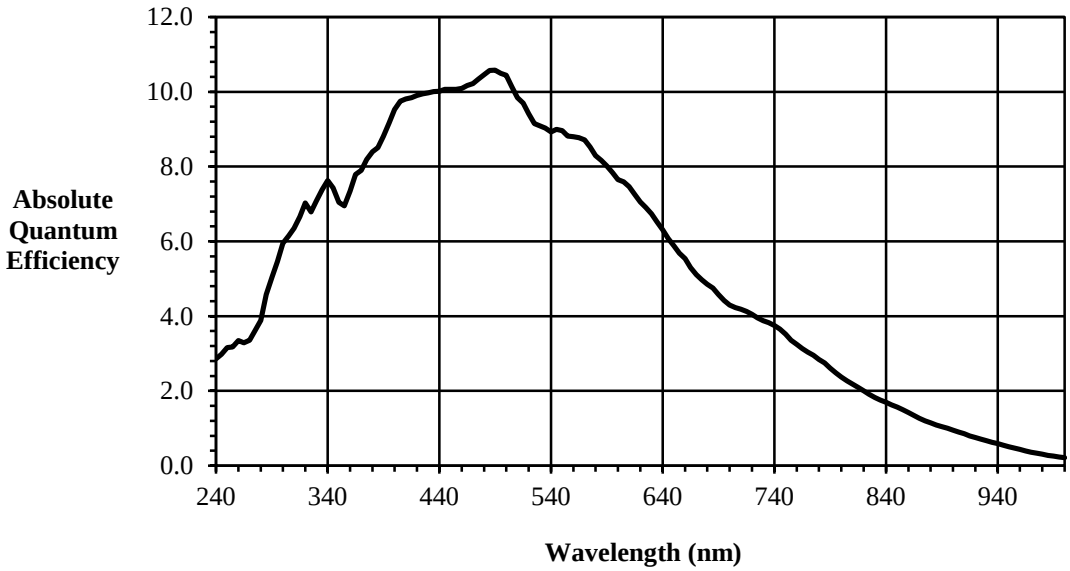


Figure 10: Monochrome without Microlens Quantum Efficiency

Color (Bayer RGB) with Microlens

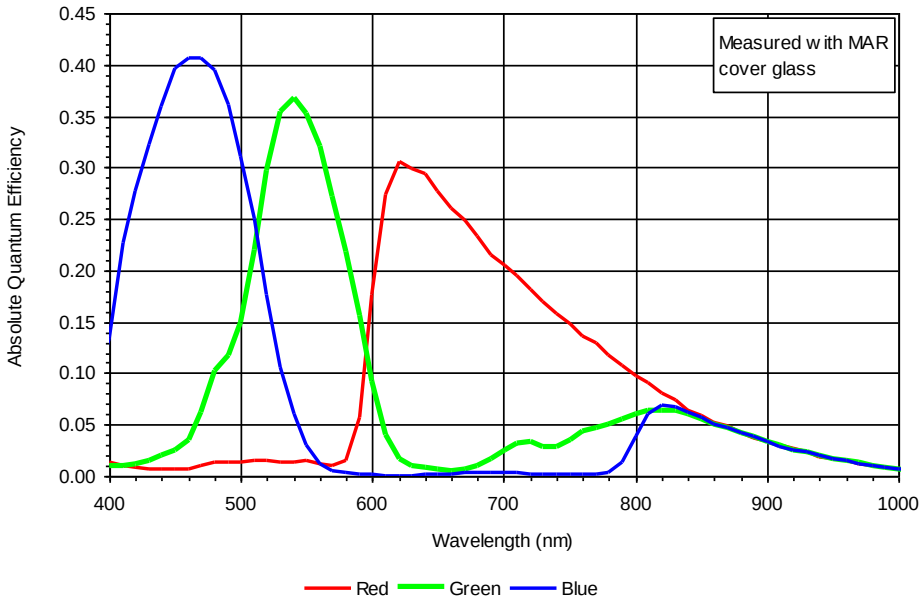


Figure 11: Color with Microlens Quantum Efficiency

ANGULAR QUANTUM EFFICIENCY

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.

For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

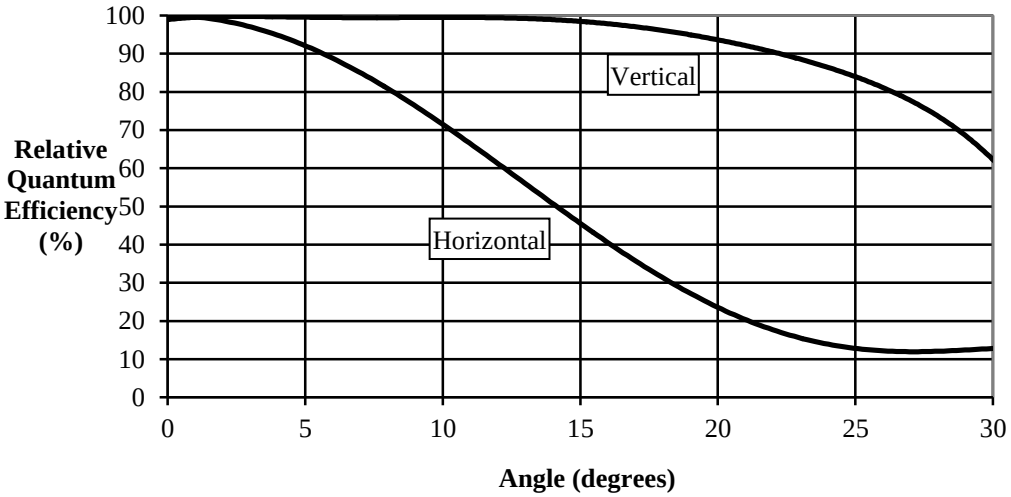


Figure 12: Angular Quantum Efficiency

DARK CURRENT VERSUS TEMPERATURE

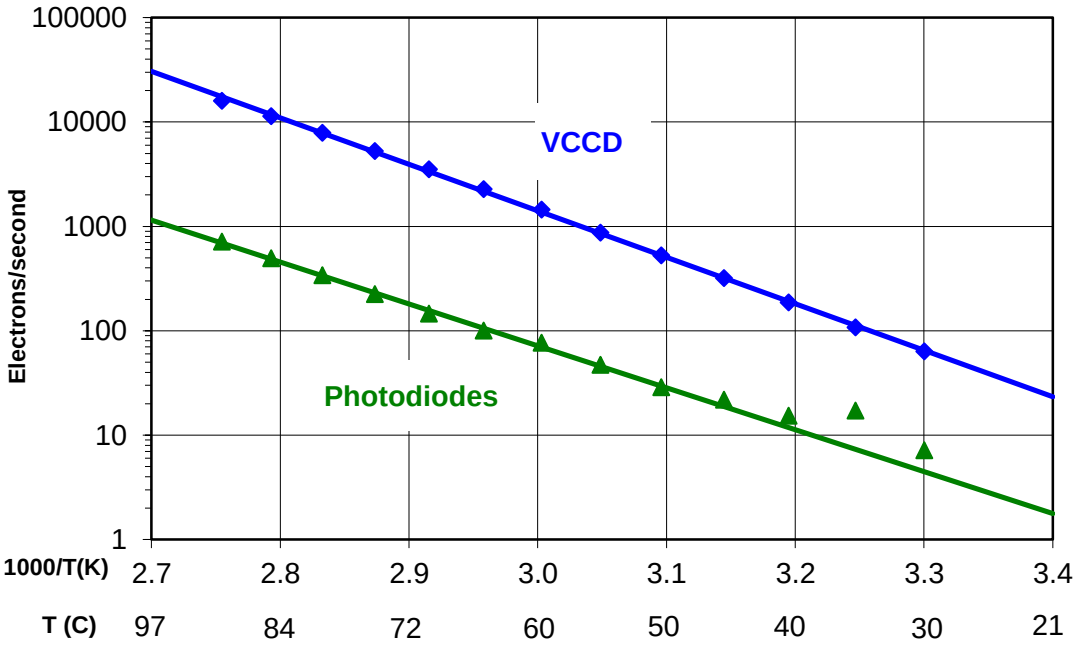


Figure 13: Dark Current versus Temperature

POWER – ESTIMATED

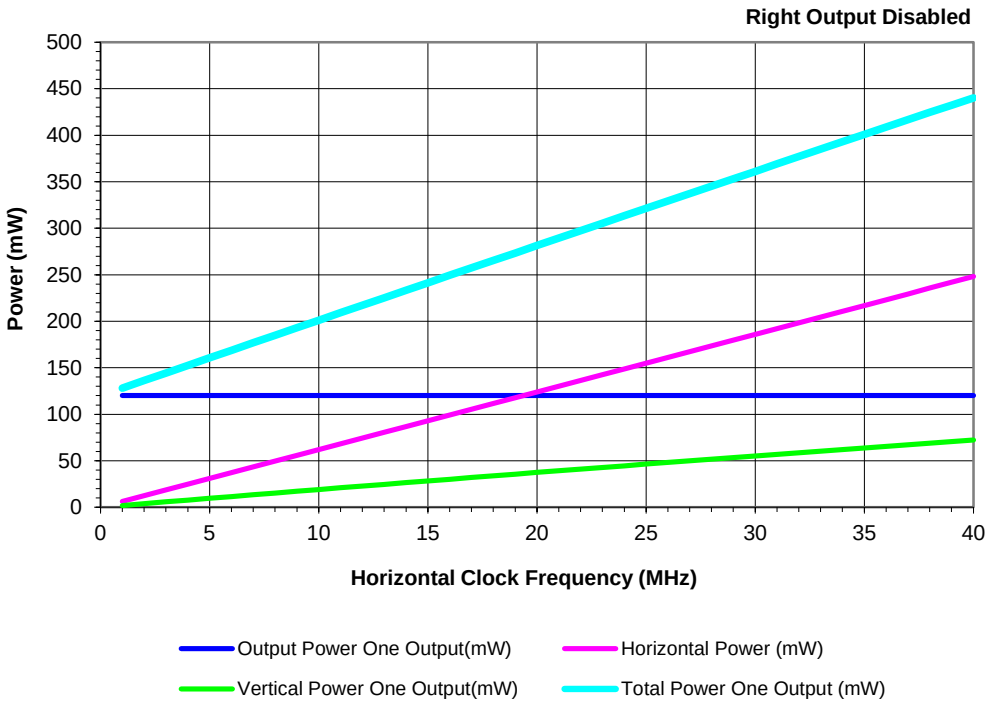


Figure 14: Power

FRAME RATES

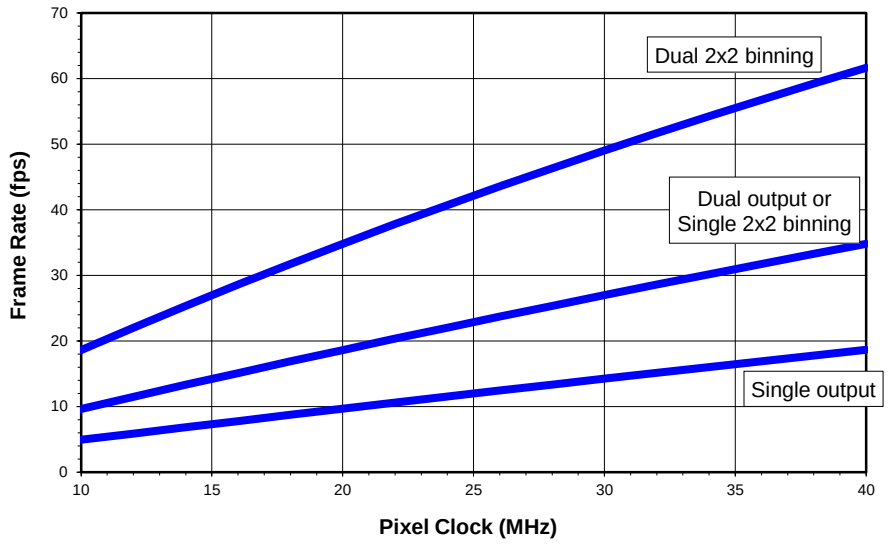


Figure 15: Frame Rates

Defect Definitions

Operational Conditions

Unless otherwise noted, the Defect Specifications are measured using the following conditions:

Description	Condition	Notes
Frame time	237 msec	1
Horizontal clock frequency	10 MHz	
Light Source (LED)	Continuous red, green and blue illumination centered at 450, 530 and 650 nm	2, 3
Operation	Nominal operating voltages and timing	

Notes:
1. Electronic shutter is not used. Integration time equals frame time.
2. LEDs used: Blue: Nichia NLPB500, Green: Nichia NSPG500S and Red: HP HLMP-8115.
3. For monochrome sensor, only green LED used.

Specifications

Description	Definition	Maximum	Temperature(s) tested at (°C)	Notes
Major dark field defective pixel	Defect ≥ 74 mV	20	27, 40	1
Major bright field defective pixel	Defect ≥ 10%			1
Minor dark field defective pixel	Defect ≥ 38 mV	200	27, 40	
Dead pixel	Defect ≥ 80%	2	27, 40	1
Saturated pixel	Defect ≥ 170 mV	5	27, 40	1
Cluster defect	A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defects horizontally	8	27, 40	1
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	27,40	1

Notes:
1. There will be at least two non-defective pixels separating any two major defective pixels.

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27 °C) temperature. Minor point defects are not included in the defect map. All pixels are referenced to pixel 1, 1 in the defect map.

Test Definitions

Test Regions of Interest

Active Area ROI: Pixel (1, 1) to Pixel (1600, 1200)

Center 100 by 100 ROI: Pixel (750, 550) to Pixel (849, 649)

Only the active pixels are used for performance and defect tests.

OverClocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 16 for a pictorial representation of the regions.

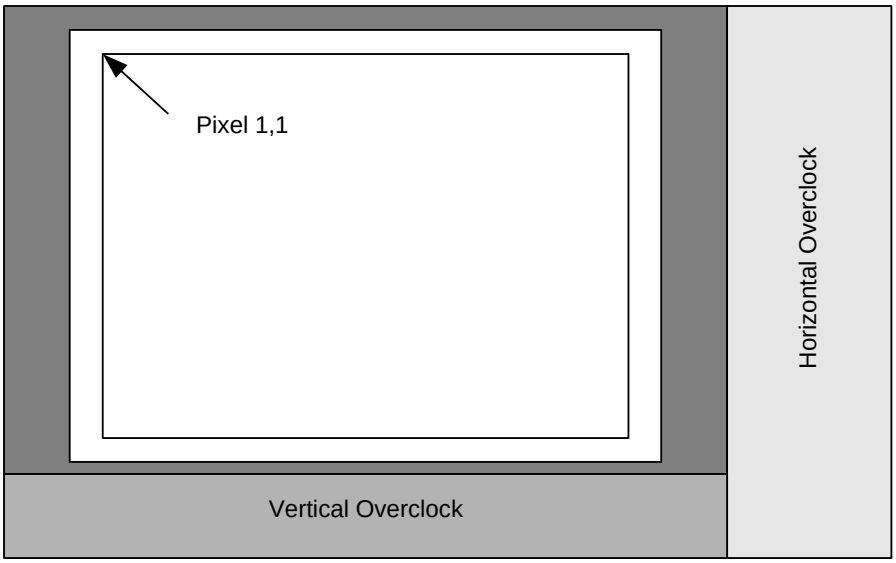


Figure 16: Overclock Regions of Interest

TESTS

Dark Field Center Uniformity

This test is performed under dark field conditions. Only the center 100 by 100 pixels of the sensor are used for this test - pixel (750, 550) to pixel (849, 649).

$$\text{Dark field center uniformity} = \text{Standard Deviation of center 100 by 100 pixels in electrons} * \left(\frac{\text{DPS Integration time}}{\text{Actual integration time used}} \right)$$

Units: e^- rms. DPS integration time: Device Performance Specification Integration Time = 33 msec.

Dark Field Global Uniformity

This test is performed under dark field conditions. The sensor is partitioned into 192 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 17. The average signal level of each of the 192 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in ADU – Horizontal overclock average in ADU) * mV per count

Where i = 1 to 192. During this calculation on the 192 sub regions of interest, the maximum and minimum signal levels are found. The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

Units: mVpp (millivolts peak to peak).

Global Uniformity

This test is performed with the imager illuminated to a level such that the output is at 80% of saturation (approximately 32,000 electrons). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 40,000 electrons. Global uniformity is defined as:

$$\text{Global Uniformity} = 100 \times \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}} \right)$$

Units: %rms. Active Area Signal = Active Area Average – Horizontal Overclock Average.

Global Peak to Peak Uniformity

This test is performed with the imager illuminated to a level such that the output is at 80% of saturation (approximately 32,000 electrons). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 40,000 electrons. The sensor is partitioned into 192 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 17. The average signal level of each of the 192 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in ADU – Horizontal overclock average in ADU) * mV per count

Where i = 1 to 192. During this calculation on the 192 sub regions of interest, the maximum and minimum signal levels are found. The global peak to peak uniformity is then calculated as:

$$\text{Global Uniformity} = \frac{\text{Maximum Signal - Minimum Signal}}{\text{Active Area Signal}}$$

Units: %pp.

Center Uniformity

This test is performed with the imager illuminated to a level such that the output is at 80% of saturation (approximately 32,000 electrons). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 40,000 electrons. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels of the sensor (see Figure 17). Center uniformity is defined as:

$$\text{Center ROI Uniformity} = 100 * \left(\frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}} \right)$$

Units: %rms. Center ROI Signal = Center ROI Average – Horizontal Overclock Average.

Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 192 sub regions of interest, each of which is 100 by 100 pixels in size (see Figure 17). In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in "Defect Definitions" section.

Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at 80% of saturation (approximately 32,000 electrons). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 40,000 electrons. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal * threshold

Bright defect threshold = Active Area Signal * threshold

The sensor is then partitioned into 192 sub regions of interest, each of which is 100 by 100 pixels in size (see Figure 17). In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 960 mV (32,000 electrons).
- Dark defect threshold: 960mV * 10% = 96 mV
- Bright defect threshold: 960mV * 10% = 96 mV
- Region of interest #1 selected. This region of interest is pixels 1,1 to pixels 100,100.
    - Median of this region of interest is found to be 960 mV.
    - Any pixel in this region of interest that is ≥ (960+96 mV) 1056 mV in intensity will be marked defective.
    - Any pixel in this region of interest that is ≤ (960-96 mV) 864 mV in intensity will be marked defective.
- All remaining 191 sub regions of interest are analyzed for defective pixels in the same manner.

TEST SUB REGIONS OF INTEREST

Pixel (1,1)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96
97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112
113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128
129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144
145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160
161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176
177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192

Pixel (1600,1200)

Figure 17: Test Sub Regions of Interest

Operation

Absolute Maximum Ratings

Description	Symbol	Minimum	Maximum	Units	Notes
Temperature	T_{OP}	-50	70	°C	1
Humidity	RH	5	90	%	2
Output Bias Current	Iout	0.0	10.0	mA	3
Off-chip Load	C_L		10	pF	4

Notes:
1. Noise performance will degrade at higher temperatures.
2. T=25 °C. Excessive humidity will degrade MTTF.
3. Total for both outputs. Current is 5 mA for each output. Note that the current bias affects the amplifier bandwidth.
4. With total output load capacitance of CL = 10pF between the outputs and AC ground.
5. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged.

Maximum Voltage Ratings Between Pins

Description	Minimum	Maximum	Units	Notes
RL, RR, H1SL, H1SR, H2SL, H2SR, H1BL, H1BR, H2BL, H2BR, OGL, OGR to ESD	0	17	V	
Pin to Pin with ESD Protection	-17	17	V	1
VDDL, VDDR to GND	0	25	V	

Notes:
1. Pins with ESD protection are: RL, RR, H1SL, H1SR, H2SL, H2SR, H1BL, H2BL, H1BR, H2BR, OGL and OGR.

DC Bias Operating Conditions (for < 40,000 electrons)

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Output Gate	OG	-2.5	-2.0	-1.5	V	1 µA	4
Reset Drain	RD	11.5	12.0	12.5	V	1 µA	5
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	1 mA	1
Ground	GND		0.0		V		
Substrate	SUB	8.0	Vab	17.0	V		2, 6
ESD Protection	ESD	-8.0	-7.0	-6.0	V		3
Output Amplifier Return	VSS	0.0	0.7	1.0	V		

Notes:

1. One output, unloaded
2. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The shipping container will be marked with two VAB voltages. One VAB will be for a 600 mV charge capacity (for operation of the horizontal clock frequencies greater than 20 MHz) and the other VAB will be for 1200 mV charge capacity (for horizontal clock frequencies at or below 20 MHz).
3. VESD must be at least 1 Volt more negative than H1L, H2L and RL during sensors operation AND during camera power turn on.
4. Output gate voltage must be set to –3 V for 40,000 - 80,000 electrons output in summed interlaced or binning modes.
5. Reset Drain voltage must be set to 13 V for 80,000 electrons output in summed interlaced or binning modes.
6. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

AC Operating Conditions

Clock Levels

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Vertical CCD Clock High	V2H	7.5	8.0	8.5	V	
Vertical CCD Clocks Midlevel	V1M, V2M	-0.2	0.0	0.2	V	
Vertical CCD Clocks Low	V1L, V2L	-9.5	-9.0	-8.5	V	
Horizontal CCD Clocks Amplitude	H1H, H2H	4.5	5.0	5.5	V	
Horizontal CCD Clocks Low	H1L, H2L	-5.0	-4.0	-3.8	V	
Reset Clock Amplitude	RH		5.0		V	1
Reset Clock Low	RL	-4.0	-3.5	-3.0	V	
Electronic Shutter Voltage	Vshutter	44	48	52	V	2
Fast Dump High	FDH	4.8	5.0	5.2	V	
Fast Dump Low	FDL	-9.5	-9	-8	V	

Notes:
1. Reset amplitude must be set to 7.0 V for 40,000 – 80,000 electrons output in summed interlaced or binning modes.
2. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

Clock Line Capacitances

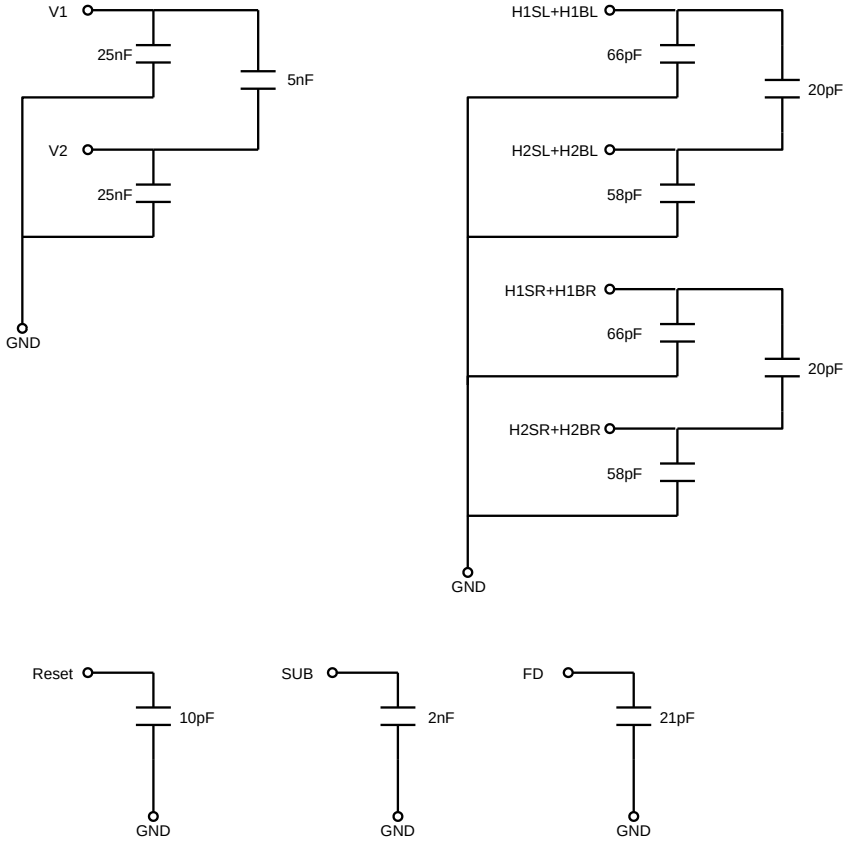


Figure 18: Clock Line Capacitances

Timing

Requirements and Characteristics

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
HCCD Delay	T_{HD}	1.3	1.5	10.0	µs	
VCCD Transfer time	T_{VCCD}	1.3	1.5	20.0	µs	
Photodiode Transfer time	T_{V3rd}	8.0	12.0	15.0	µs	
VCCD Pedestal time	T_{3P}	20.0	25.0	50.0	µs	
VCCD Delay	T_{3D}	15.0	20.0	100.0	µs	
Reset Pulse time	T_{R}	5.0	10.0		ns	
Shutter Pulse time	T_{S}	3.0	5.0	10.0	µs	
Shutter Pulse delay	T_{SD}	1.0	1.6	10.0	µs	
HCCD Clock Period	T_{H}	25.0	50.0	200.0	ns	
VCCD rise/fall time	T_{VR}	0.0	0.1	1.0	µs	
Fast Dump Gate delay	T_{FD}	0.0		0.5	µs	
Vertical Clock Edge Alignment	T_{VE}	0.0		100.0	ns	

TIMING MODES

Progressive Scan

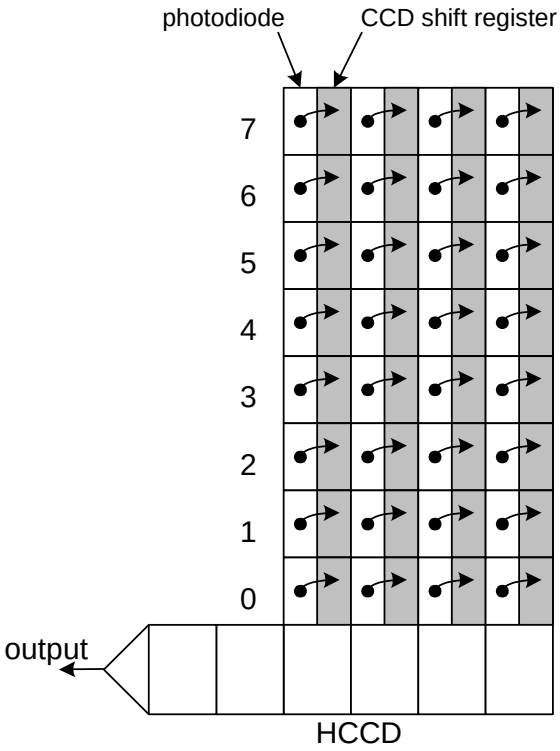


Figure 19: Progressive Scan Operation

In progressive scan read out every pixel in the image sensor is read out simultaneously. Each charge packet is transferred from the photodiode to the neighboring vertical CCD shift register simultaneously. The maximum useful signal output is limited by the photodiode charge capacity to 40,000 electrons.

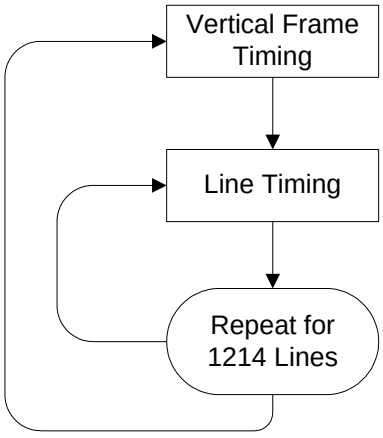


Figure 20: Progressive Scan Flow Chart

FRAME TIMING

Frame Timing without Binning – Progressive Scan

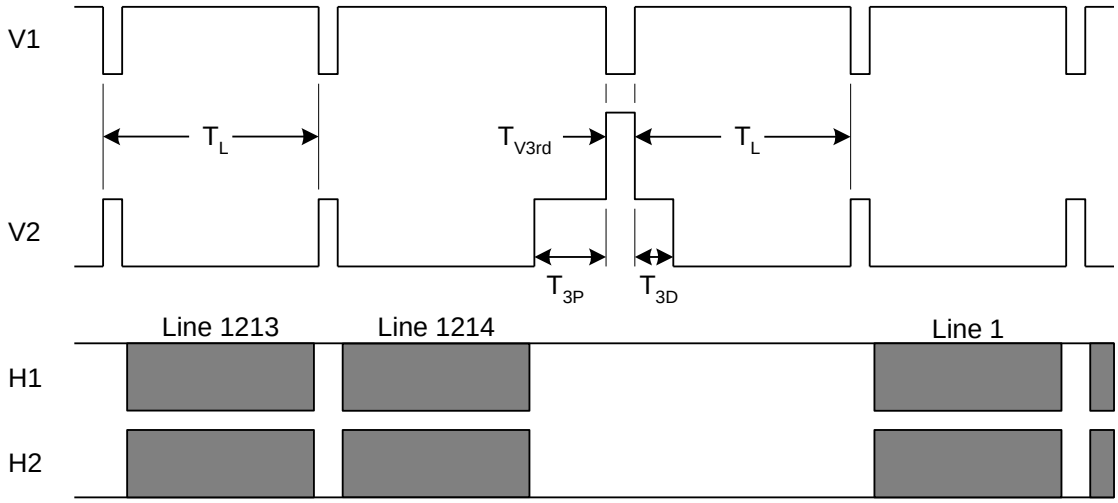


Figure 21: Framing Timing without Binning

Frame Timing for Vertical Binning by 2 – Progressive Scan

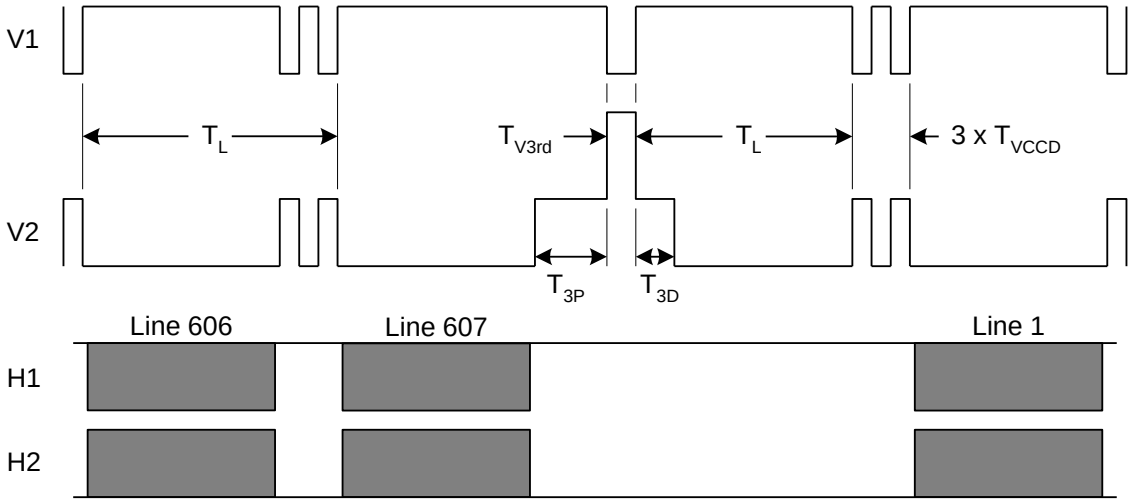


Figure 22: Frame Timing for Vertical Binning by 2

Frame Timing Edge Alignment

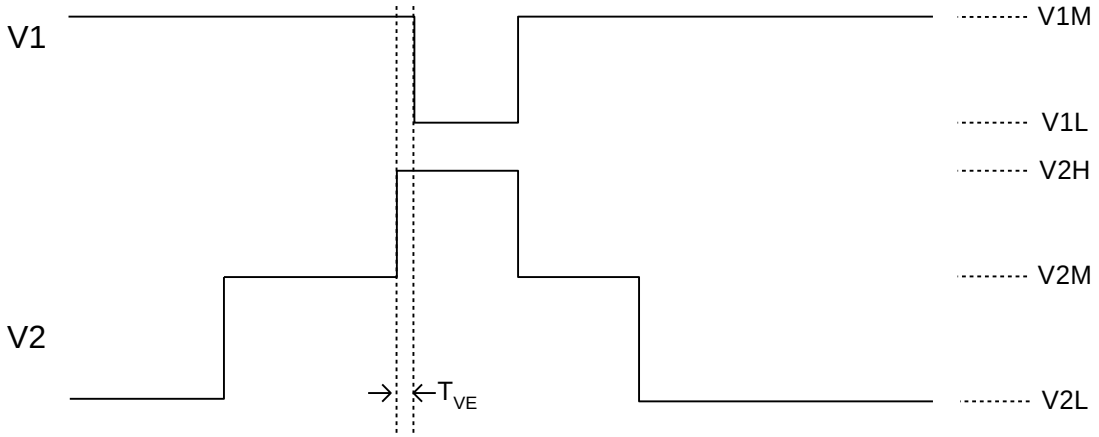


Figure 23: Frame Timing Edge Alignment

LINE TIMING

Line Timing Single Output- Progressive Scan

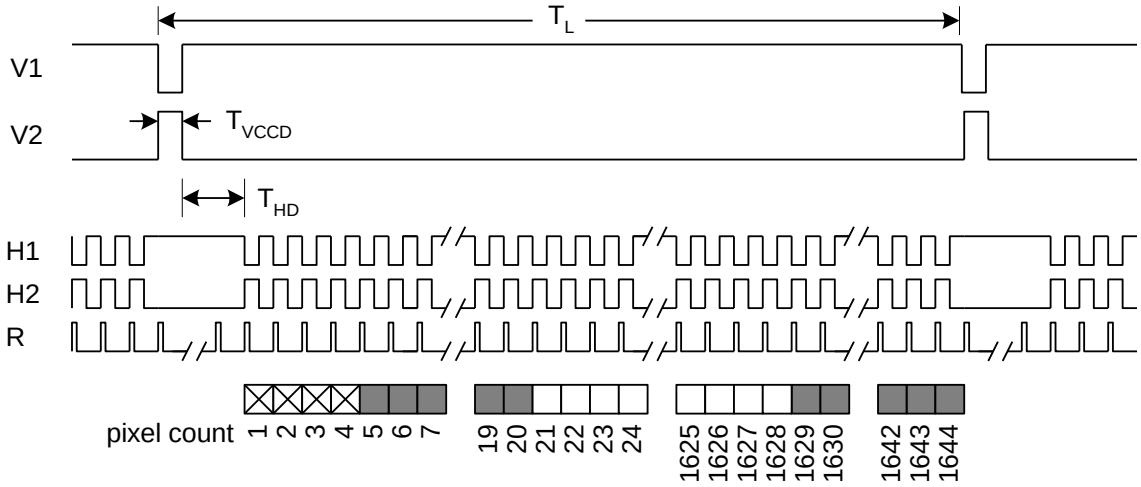


Figure 24: Line Timing Single Output

Line Timing Dual Output – Progressive Scan

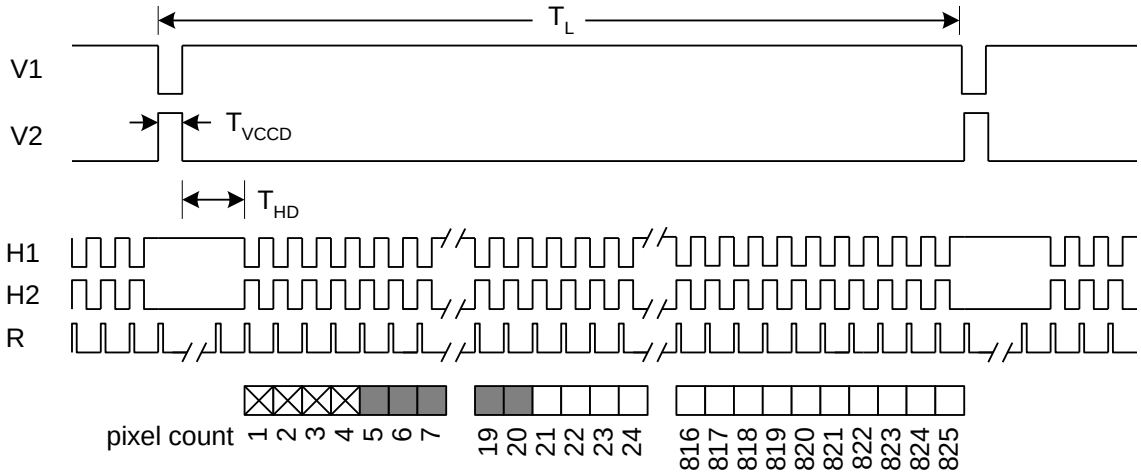


Figure 25: Line Timing Dual Output

Line Timing Vertical Binning by 2 – Progressive Scan

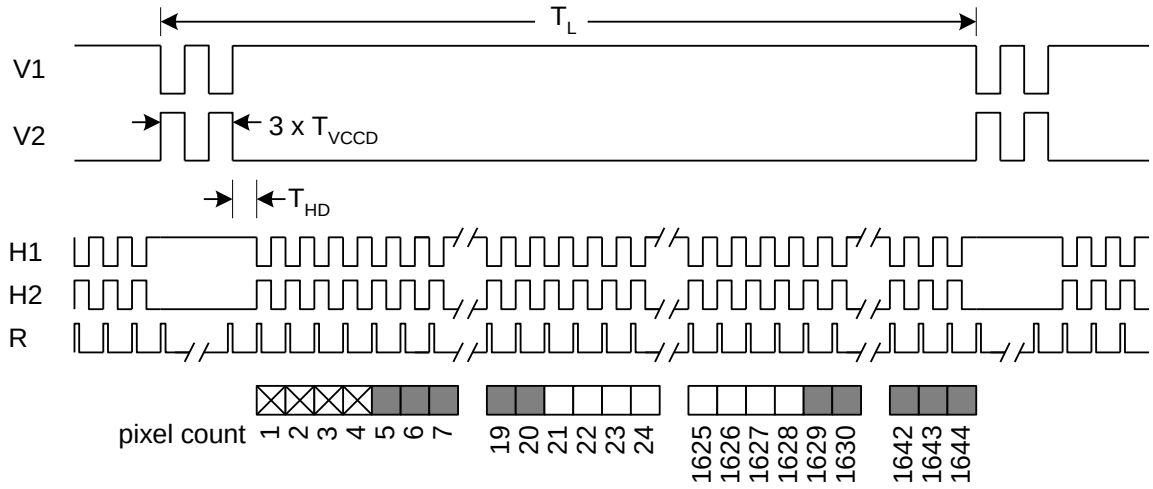


Figure 26: Line Timing Vertical Binning by 2

Line Timing Detail – Progressive Scan

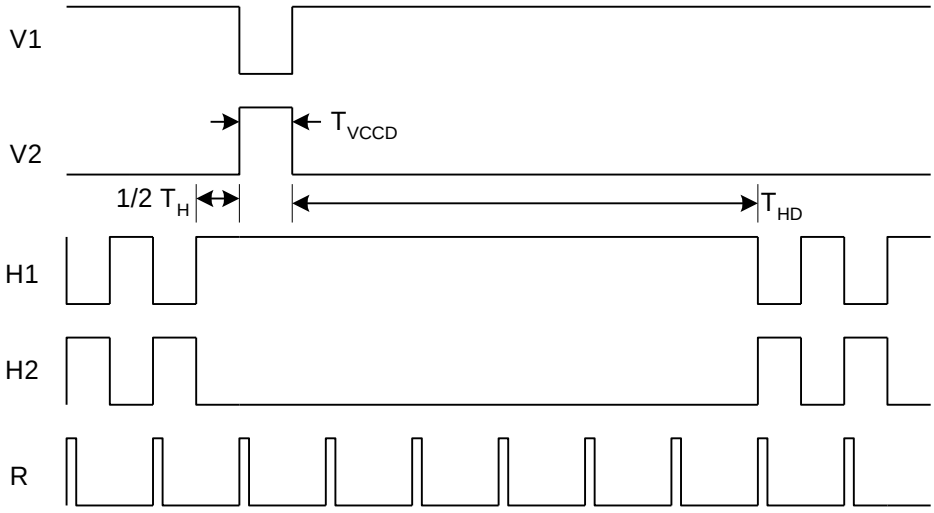


Figure 27: Line Timing Detail

Line Timing Binning by 2 Detail – Progressive Scan

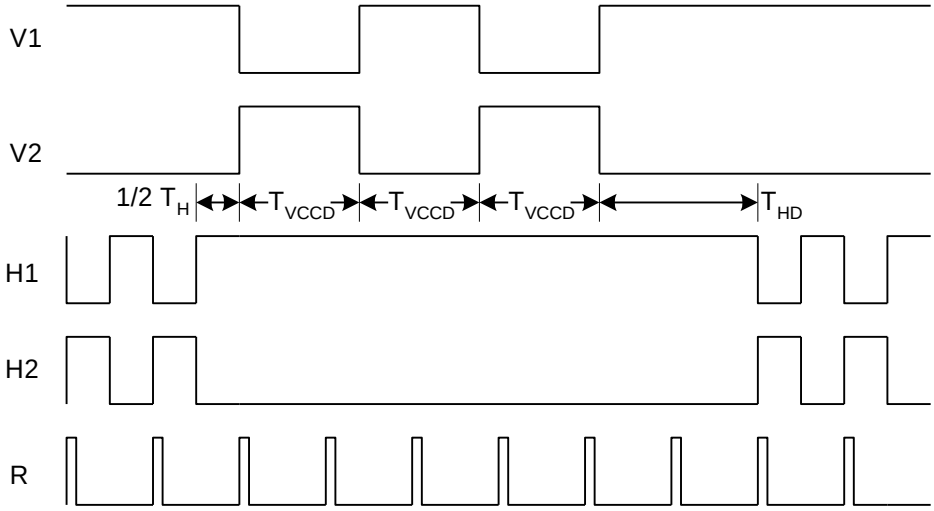


Figure 28: Line Timing by 2 Detail

Line Timing Edge Alignment

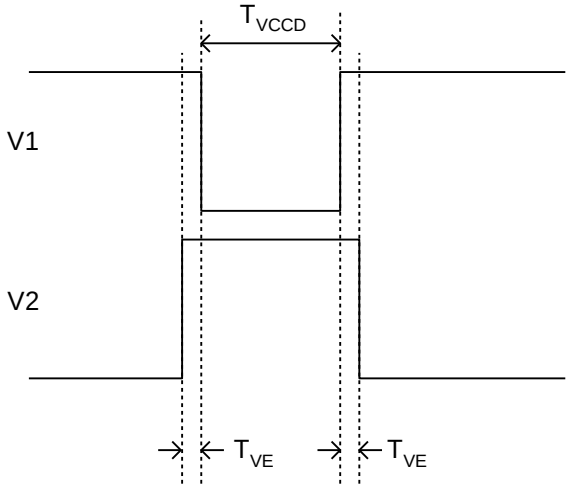


Figure 29: Line Timing Edge Alignment

Pixel Timing

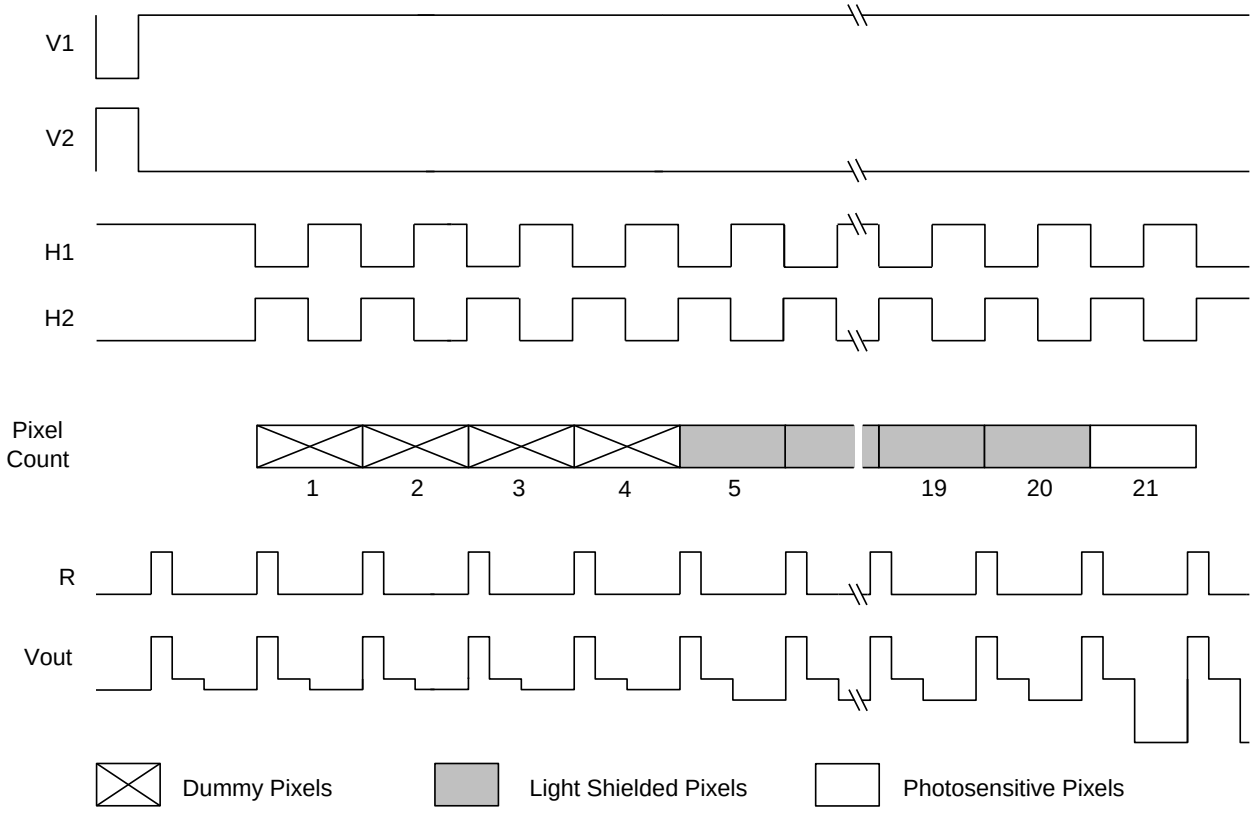


Figure 30: Pixel Timing

Pixel Timing Detail

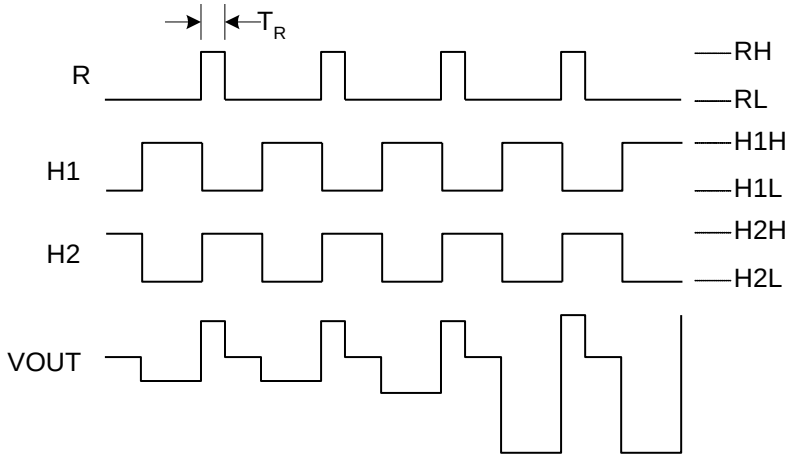


Figure 31: Pixel Timing Detail

FAST LINE DUMP TIMING

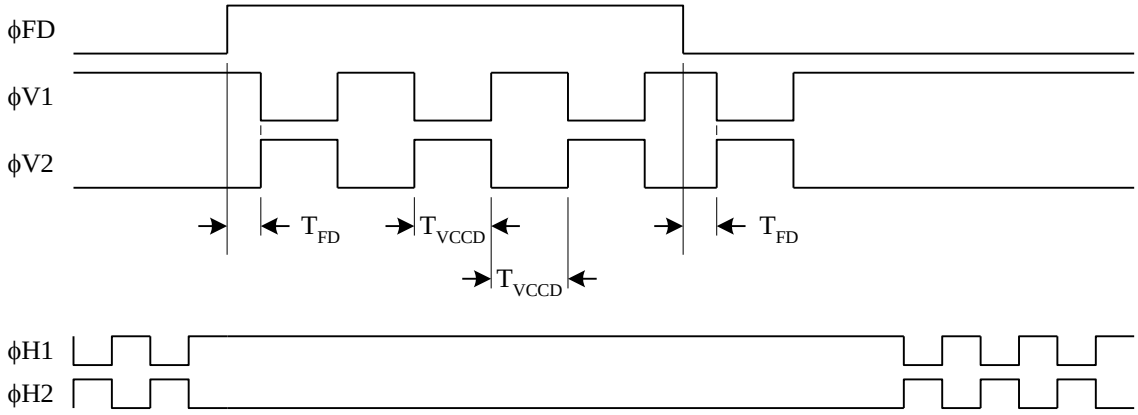


Figure 32: Fast Line Dump Timing

ELECTRONIC SHUTTER

Electronic Shutter Line Timing

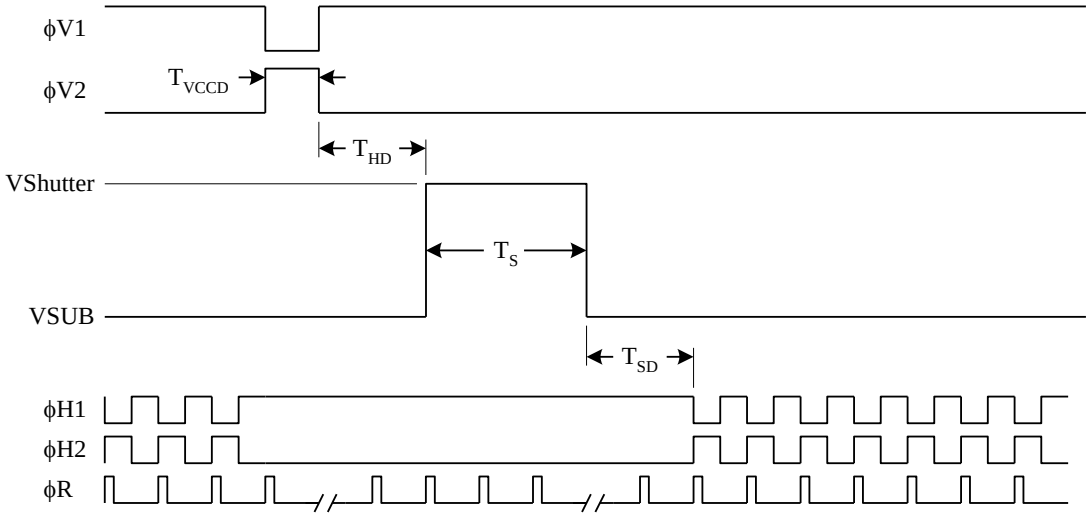


Figure 33: Electronic Shutter Line Timing

Electronic Sutter – Integration Time Definition

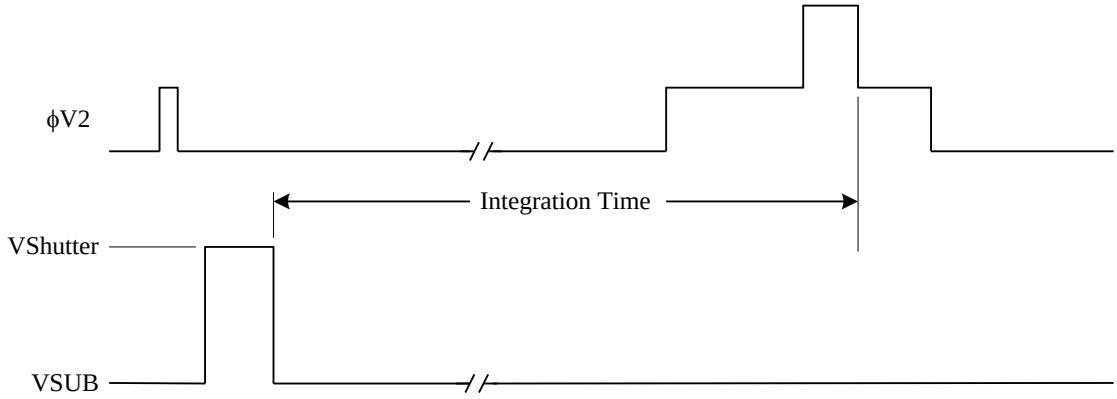
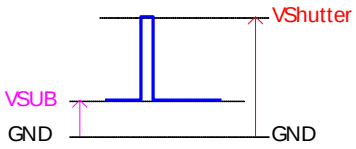


Figure 34: Integration Time Definition

Electronic Shutter – DC and AC Bias Definition

The figure below shows the DC bias (VSUB) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.



Electronic Shutter Description

The voltage on the substrate (SUB) determines the charge capacity of the photodiodes. When SUB is 8 volts the photodiodes will be at their maximum charge capacity. Increasing VSUB above 8 volts decreases the charge capacity of the photodiodes until 48 volts when the photodiodes have a charge capacity of zero electrons. Therefore, a short pulse on SUB, with a peak amplitude greater than 48 volts, empties all photodiodes and provides the electronic shuttering action.

It may appear the optimal substrate voltage setting is 8 volts to obtain the maximum charge capacity and dynamic range. While setting VSUB to 8 volts will provide the maximum dynamic range, it will also provide the minimum antiblooming protection.

The KAI-2020 VCCD has a charge capacity of 50,000 electrons (50 ke^-). If the SUB voltage is set such that the photodiode holds more than 50 ke^-, then when the charge is transferred from a full photodiode to VCCD, the VCCD will overflow. This overflow condition manifests itself in the image by making bright spots appear elongated in the vertical direction. The size increase of a bright spot is called blooming when the spot doubles in size. The blooming can be eliminated by increasing the voltage on SUB to lower the charge capacity of the photodiode. This ensures the VCCD charge capacity is greater than the photodiode capacity. There are cases where an extremely bright spot will still cause blooming in the VCCD. Normally, when the photodiode is full, any additional electrons generated by photons will spill out of the photodiode. The excess electrons are drained harmlessly out to the substrate. There is a maximum rate at which the electrons can be drained to the substrate. If that maximum rate is exceeded, (for example, by a very bright light source) then it is possible for the total amount of charge in the photodiode to exceed the VCCD capacity. This results in blooming. The amount of antiblooming protection also decreases when the integration time is decreased. There is a compromise between photodiode dynamic range (controlled by VSUB) and the amount of antiblooming protection. A low VSUB voltage provides the maximum dynamic range and minimum (or no) antiblooming protection. A high VSUB voltage provides lower dynamic range and maximum antiblooming protection. The optimal setting of VSUB is written on the container in which each KAI-2020 is shipped. The given VSUB voltage for each sensor is selected to provide antiblooming protection for bright spots at least 100 times saturation, while maintaining at least 40 ke- of dynamic range.

The electronic shutter provides a method of precisely controlling the image exposure time without any mechanical components. If an integration time of T_{INT} is desired, then the substrate voltage of the sensor is pulsed to at least 40 volts T_{INT} seconds before the photodiode to VCCD transfer pulse on V2. Use of the electronic shutter does not have to wait until the previously acquired image has been completely read out of the VCCD.

LARGE SIGNAL OUTPUT

When the image sensor is operated in the binned or summed interlaced modes there will be more than 20,000 electrons in the output signal. The image sensor is designed with a 30 μV/e charge to voltage conversion on the output. This means a full signal of 40,000 electrons will produce a 600 mV change on the output amplifier. The output amplifier was designed to handle an output swing of 600 mV at a pixel rate of 40 MHz. If 40,000 electron charge packets are generated in the binned or summed interlaced modes then the output amplifier output will have to swing 1200 mV. The output amplifier does not have enough bandwidth (slew rate) to handle 1200 mV at 40 MHz. Hence, the pixel rate will have to be reduced to 20 MHz if the full dynamic range of 40,000 electrons is desired.

The charge handling capacity of the output amplifier is also set by the reset clock voltage levels. The reset clock driver circuit is very simple if an amplitude of 5 V is used. But the 5 V amplitude restricts the output amplifier charge capacity to 20,000 electrons. If the full dynamic range of 40,000 electrons is desired then the reset clock amplitude will have to be increased to 7 V.

If you only want a maximum signal of 20,000 electrons in binned or summed interlaced modes, then a 40 MHz pixel rate with a 5 V reset clock may be used. The output of the amplifier will be unpredictable above 20,000 electrons so be sure to set the maximum input signal level of your analog to digital converter to the equivalent of 20,000 electrons (600 mV).

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-55	80	°C	1
Humidity	RH	5	90	%	2

Notes:
1. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
2. T=25 °C. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Drawings

COMPLETED ASSEMBLY

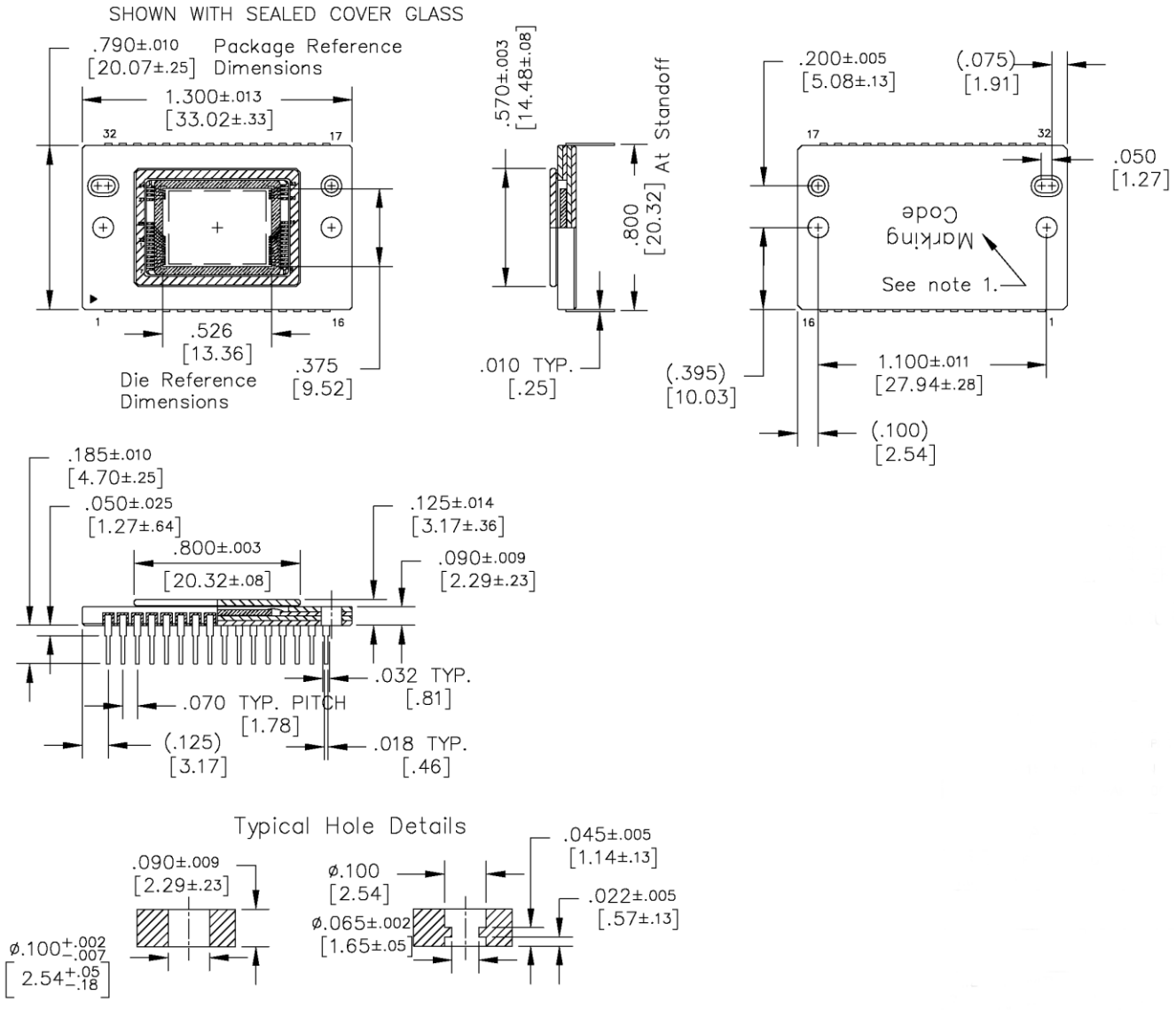
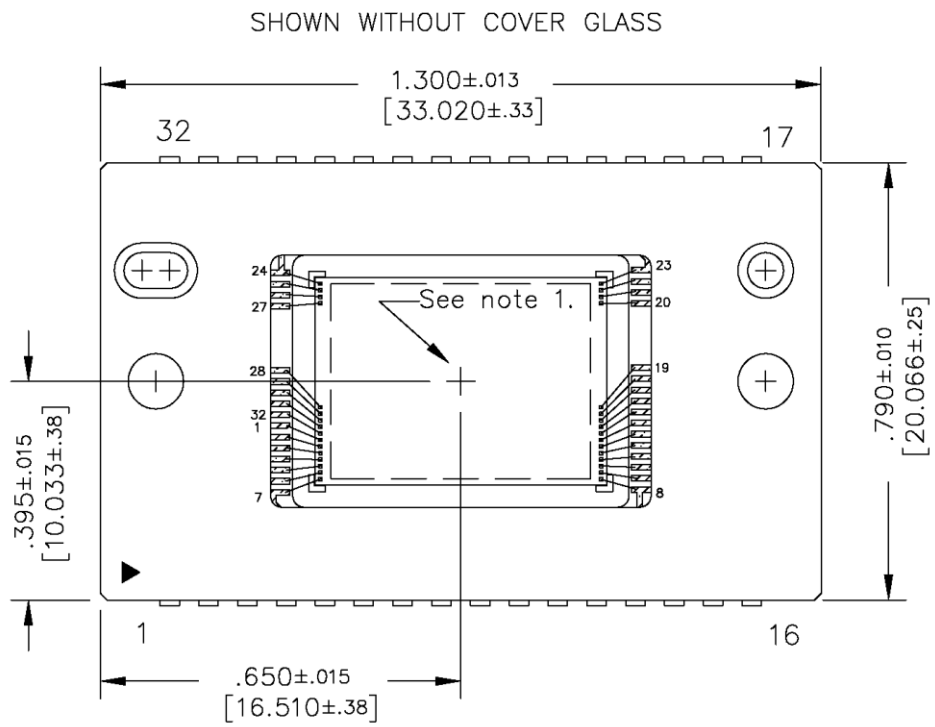


Figure 35: Completed Assembly (1 of 2)

Notes:

1. See Ordering Information for marking code
2. Cover glass is manually placed and visually aligned over die – location accuracy is not guaranteed.
3. Dimension units: INCH [MM]
4. Tolerance: Unless otherwise specified
    a. Ceramic ±1% no less than 0.005”
    b. L/F ±1% no more than 0.005”



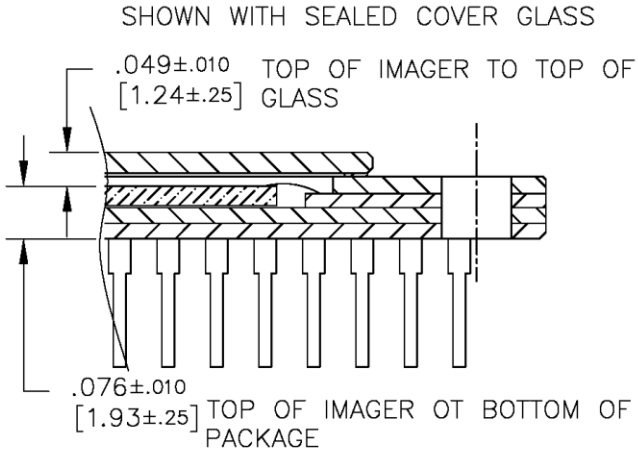
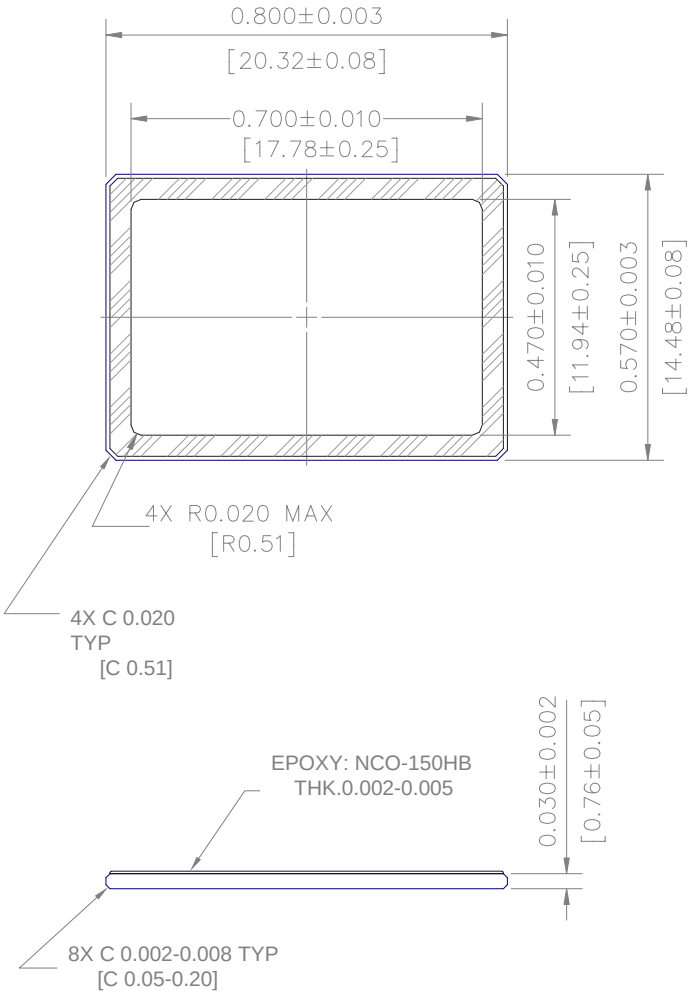


Figure 36: Completed Assembly (2 of 2)

Notes:

1. Center of image is offset from center of package by (0.00, 0.00)mm nominal.
2. Die is aligned within 2 degree of any package cavity edge.
3. Dimension units: INCH [MM]
4. Tolerance: Unless otherwise specified
    a. Ceramic ±1% no less than 0.005”
    b. L/F ±1% no more than 0.005”

Cover Glass



NOTES:
1. MATERIALS: SUBSTRATE = SCHOTT D263T eco or equivalent
EPOXY = NCO-150HB
THK = 0.002 - 0.005
2. DUST/SCRATCH COUNT = 10 MICRON MAX
3. DOUBLE SIDED AR COATING REFLECTANCE:
420 - 435 nm < 2.0%
435 - 630 nm < 0.8%
630 - 680 nm < 2.0%

UNITS: IN [MM]
TOLERANCE: UNLESS OTHERWISE SPECIFIED
+/- 1% NO LESS THAN 0.005"

Figure 37: Glass Drawing

GLASS TRANSMISSION

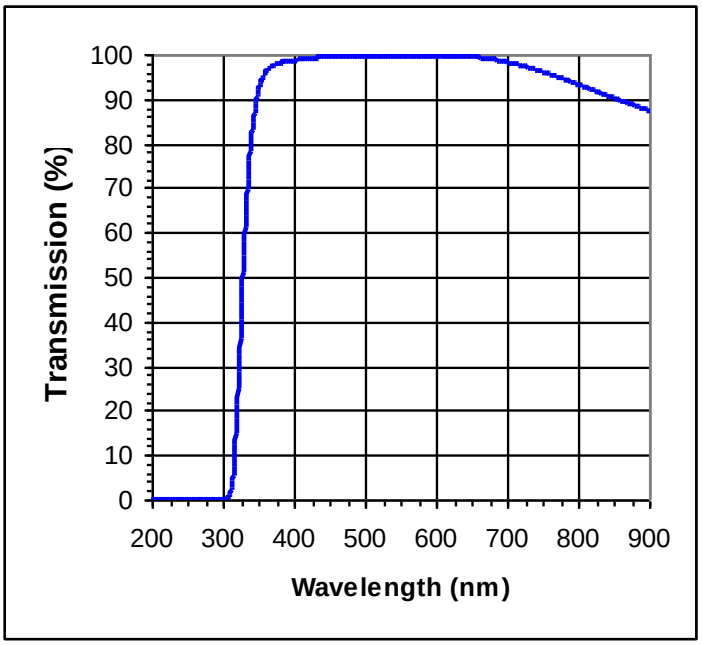


Figure 38: MAR Glass Transmission

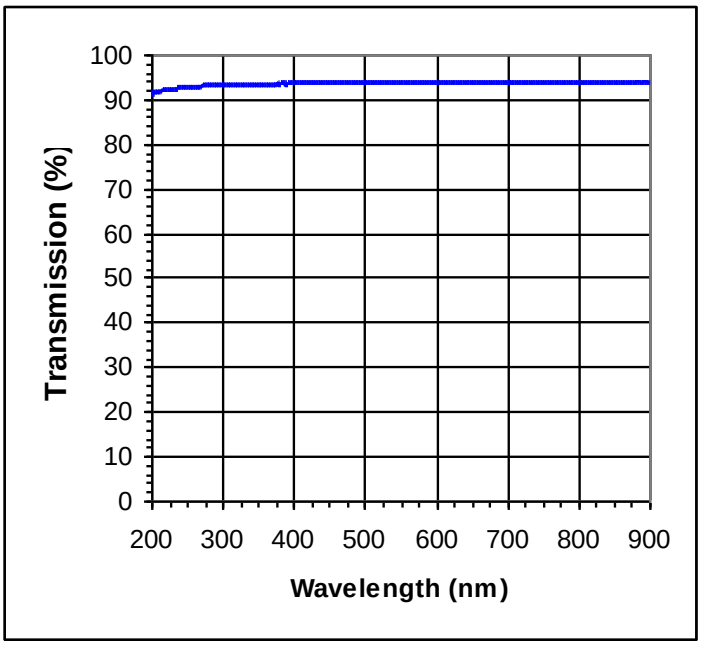


Figure 39: Quartz Glass Transmission

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

MTD/PS-0692

Revision Number	Description of Changes
1.0	• Initial release. Same as rev. F (preliminary)
2.0	• Peak QE table – swapped Red and Blue titles to match wavelength • Defect Definitions – tightened limits for major dark field (358mV to 74mV), major dark field (15% to 10%), and minor dark field (114mV to 38mV). Added Dead pixel and Saturated pixels definitions • Test 7: updated calculations with the 10% threshold • Added maximum voltage ratings between pins table • Modified DC Operating conditions to indicate settings for < 40Ke-). Removed min and max values for GND • Timing Requirements – removed nominal value for TFD
2.1	• Removed caution for cover glass protective tape. The use of the protective tape has been discontinued.
3.0	• Updated format
4.0	• Added the note "Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*" to the following sections ○ DC Bias Operating Conditions ○ AC Operating Conditions ○ Storage and Handling • Changed cover glass material to D263T eco or equivalent

PS-0017

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections • Reorganized structure for consistency with other Interline Transfer CCD documents
1.1	• Updated branding

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